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8100

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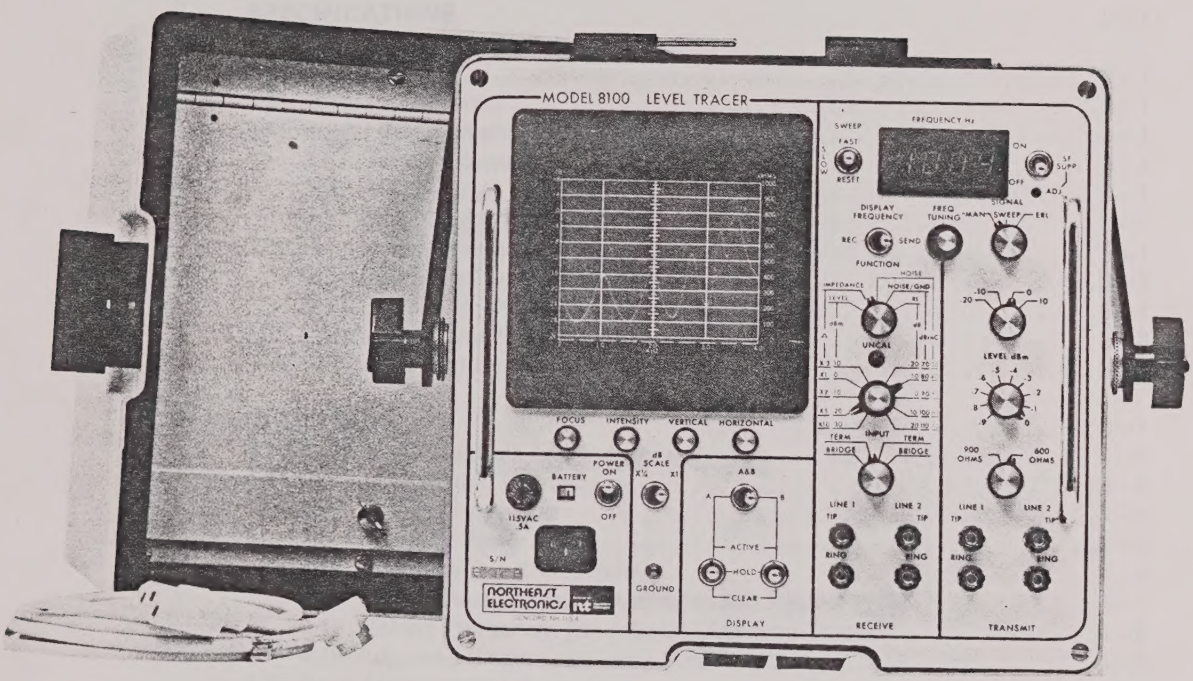
DIVISION OF tau-tron inc.
A UNIT OF GENERAL SIGNAL



NORTHEAST ELECTRONICS

MODEL 8100

LEVEL TRACER

northeast electronics
DIVISION OF tau-tron inc.
A UNIT OF GENERAL SIGNAL

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SECTION 1

GENERAL DESCRIPTION

1.1 This manual covers the Northeast Electronics Model 8100 Level Tracer. The Level Tracer is a portable instrument with multiple measurement and display capabilities. It has the features necessary for:

a. cable conformance and acceptance testing,

b. cable fault diagnosis,

c. through and terminal balancing,

d. loss and noise transmission measurements,

e. VF response alignment and equalization.

1.2 The Level Tracer consists of a transmitting section and a receiving section. The transmitting section can be swept or manually tuned across a 200 to 4000 Hz frequency range. The transmitting section also generates an echo return loss test signal per Bell requirements. The receiving section can be used separately to measure level, noise or frequency. When combined with the transmitting section, the receive section can measure loss, impedance, return loss, or echo return loss.

1.3 The transmit section provides both 600-ohm and 900-ohm source impedances essentially constant over the sweep range. The output level may be set from −29 dBm to +10 dBm in 1-dB steps. The receive section's measuring range is 80 dB for level, noise, and return loss measurements. When measuring impedance, the Level Tracer displays absolute values from a short circuit (200 ohms) to 10 kilohms.

1.4 The principle indicator is an oscilloscope-type cathode ray tube (CRT) which displays frequency on the horizontal scale and a transmission characteristic (level, noise, impedance, or return loss) on the vertical scale. The display is linear on the horizontal scale for frequency in kHz and linear on the vertical scale for levels in dB or impedance in ohms. A digital readout shows the transmitted or received frequency (as selected) with an accuracy of ±1 Hz.

1.5 Measurements can be made individually on either of two input lines, or on both input lines alternately as with a dual trace oscilloscope. Measurement data from each input line is stored in a digital memory from which the CRT traces are continuously refreshed. Thus, the Level Tracer presents two non-fading traces which can be individually updated with new measurement data . . . or can be held on screen indefinitely for reference.

1.6 This permits on-screen comparison of characteristics:

a. between two lines (for example, pairs in loaded or non-loaded cable),

b. between a line and a reference standard or an artificial cable,

c. between two sides of a line and ground.

A trace from a previous measurement can be held on screen for comparison with a new trace made after alignment, equalization, conditioning, build out, or repair.

1.7 TYPES OF TESTS

1.8 The Level Tracer may be used for straight-forward measurement of level vs frequency characteristics. The arrangement is shown in Figure 1−1A. Two Level Tracers may be used. Either a manually operated oscillator or a milliwatt test line may be substituted as the transmitting device.

1.9 In level testing, the Level Tracer receive section automatically follows the incoming frequency of a test signal. This permits convenient, hands-off testing with far end signal sources.

1.10 Precision swept or manually-tunable output signals are available from the Level Tracer's transmitting section for use in level testing. SF suppression can be selected to skip transmission over a 300-Hz band centered at any frequency from 2000 Hz to 4000 Hz. This prevents unwanted dropping (return to on hook) of a circuit under test.

1.11 For noise measurements, a quiet termination is substituted for the transmitting device as shown in Figure 1−1B. C-message noise measurements can be made on either a metallic or noise to ground basis. Noise test results appear as straight horizontal traces on the display screen.

1.12 When impedance measurements are made, the Level Tracer internal arrangement is shown in Figure 1−1C. The transmitting section and receiving section have impedance arrangements which make the output of the oscillator into a current source. Thus, the oscillator's output voltage depends upon the impedance being measured. The measuring section becomes (in effect) a voltmeter, interpreting the voltage in terms of

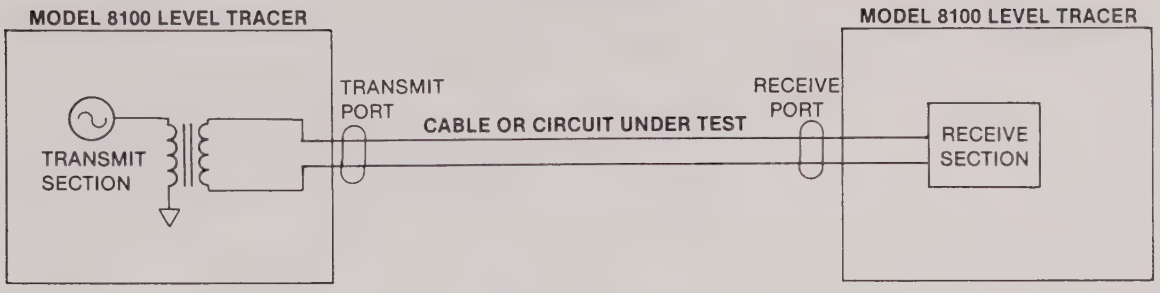
absolute impedance (magnitude only) of the circuit under test.

1.13 Figure 1—1D shows the Level Tracer arrangement when 2-wire return loss measurements are made. For these measurements, the Level Tracer becomes a bridge-type circuit. The use of gain within the receive section increases the ability to detect small imbalances. To obtain high return loss, the bridge circuit must be balanced both with respect to magnitude and phase angle of the two compared circuits.

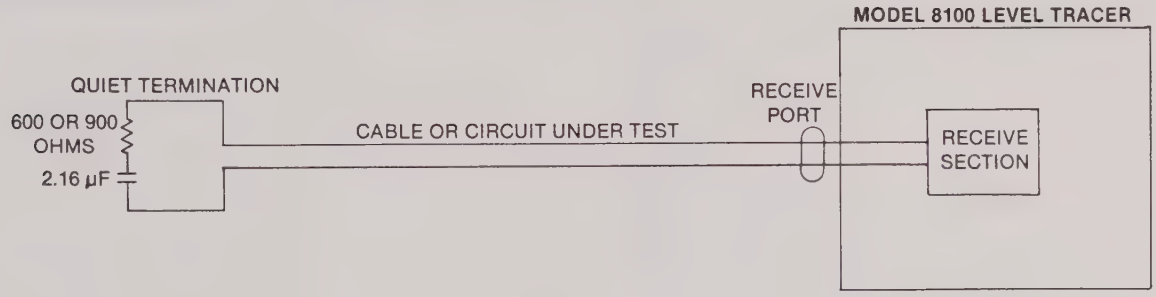
1.14 Return loss measurements can be made in several ways. The reference arm can be an artificial cable or standard cable with both the cable under test and the artificial cable terminated with precision or compromise networks. Measurements may also be made on an open circuit or short circuit basis. For structural return loss measurements, the cable under test is terminated in a precision network while the reference arm only has a precision network.

1.15 The Level Tracer may be connected as a resistance, inductance, or capacitive bridge by using a resistor, inductor or capacitor in the reference arm. During office balance or structural acceptance tests on facilities, the test signal can be an ERL (weighted noise) signal in lieu of a fixed tuned or swept signal. The simultaneous transmit and receive capabilities of the Level Tracer can be used to make return loss measurements on 4-wire circuits.

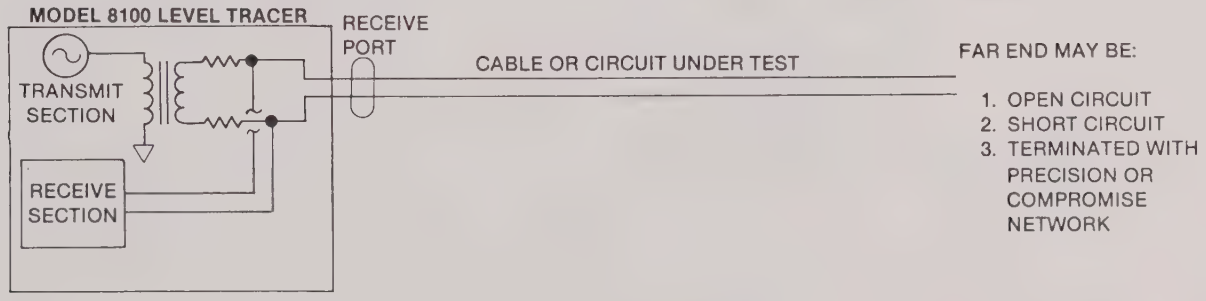
1.16 A number of graticule overlays are supplied with the Level Tracer. These overlays can be used to make permanent copies of the traces shown on the display screen.



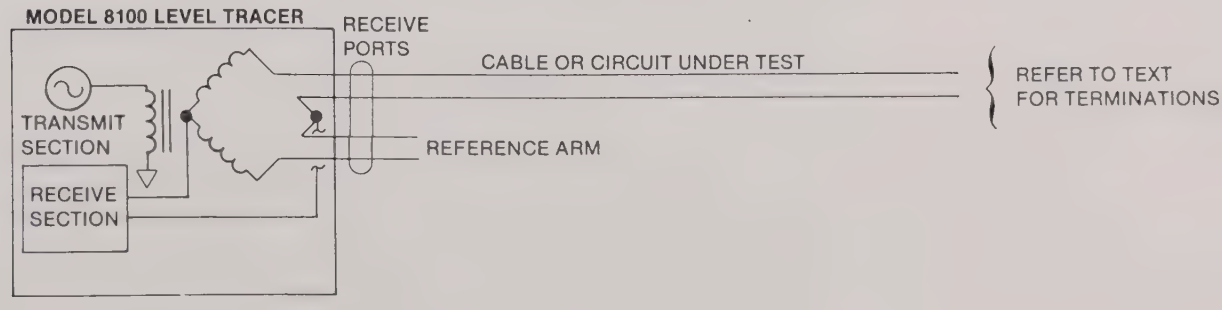
A - LEVEL MEASUREMENTS



B - NOISE MEASUREMENTS



C - IMPEDANCE MEASUREMENTS



D - RETURN LOSS MEASUREMENTS

Figure 1—1. Level Tracer Measurements

SECTION 2

SPECIFICATIONS

2.1 Major specifications of the Model 8100 Level Tracer are listed in Table 2—1. Frequency response curves for the ERL and C-message filters are shown in Figures 2—1 and 2—2.

Table 2—1. Overall Specifications.

TRANSMIT SECTION	
Frequency Range:	200 to 4000 Hz
Output Level:	−29 to +10 dBm in 1-dB steps
Output Level Accuracy:	±0.1 dB at 1 kHz ±0.1 dB from 200 to 4000 Hz, referred to 1 kHz
Sine Wave Distortion:	less than 2% worst case distortion and noise
ERL Test Signal:	weighted noise spectrum per Bell technical reference pub 41009 (See Figure 2—1)
Frequency Tuning:	sweep or manual, selectable
Sweep Time:	fast, 3 seconds per sweep or slow, 6 seconds per sweep
Outputs:	2 identical, electrically isolated output ports
RECEIVE SECTION	
LEVEL MEASUREMENTS	
Range:	−62 to +18 dBm
Accuracy:	±0.2 dB at 1 kHz
Frequency Response:	±0.1 dB from 200 to 4000 Hz
IMPEDANCE MEASUREMENTS	
Range:	0 to 10 kohms
Accuracy:	±5% of full scale - nominal ±10% of full scale - worst case
RETURN LOSS MEASUREMENTS (2-WIRE)	
Range:	up to 52 dB
Accuracy:	better than ±1 dB with a standard impedance between 300 and 1000 ohms

Table 2—1. (Cont'd)

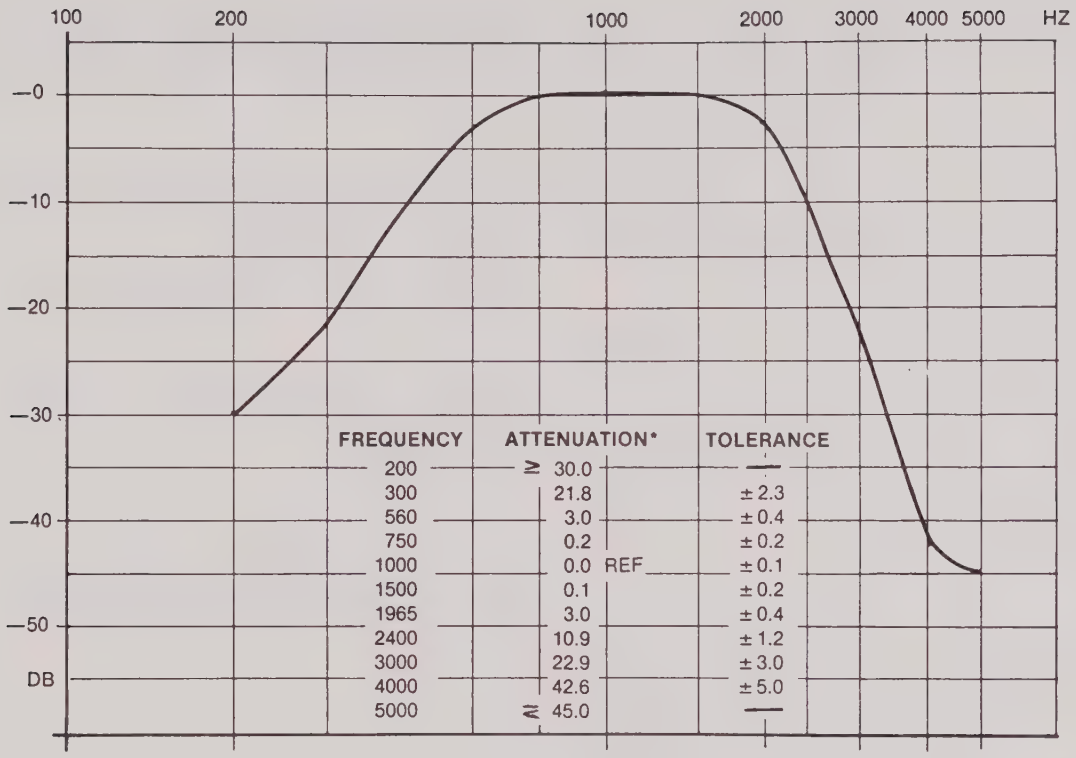
RL Test Signal:	swept or manually tuned sine wave or ERL band-limited noise
NOISE MEASUREMENTS	
Metallic Noise Range:	−2 to +78 dBrnC
Noise To Ground Range:	+38 to +118 dBrnC
Accuracy:	±1 dB
Weighting:	C-message (see Figure 2—2)
FREQUENCY MEASUREMENTS	
Range:	0 to 9999 Hz
Accuracy:	±1 Hz
Input Level:	−62 to +18 dBm
Signal To Noise Ratio:	15 dB
DISPLAY SECTION	
Type:	dual channel CRT
Modes:	A only, B only, and A & B dual display
Update:	single or continuous
Trace Refresh Rate:	about 50 times per second per trace
Frequency Marker:	shows instrument's tuning as an enhanced dot on the traces
Trace Persistence:	unlimited because of digital trace memory
Graticule Size:	7.8 x 9.6 cm (3-1/8 x 3-13/16 in)
Scales:	
Horizontal Axis:	linear 200 to 4000 Hz
Vertical Axis:	linear 0 to 1000 impedance scale linear −32 to +8 dB level/noise/return loss scale

GENERAL

INPUT/OUTPUT IMPEDANCE	
Output Impedance:	600 ± 2% ohms or 900 ± 2% ohms
Input Terminating Impedance:	600 ± 2% ohms or 900 ± 2% ohms

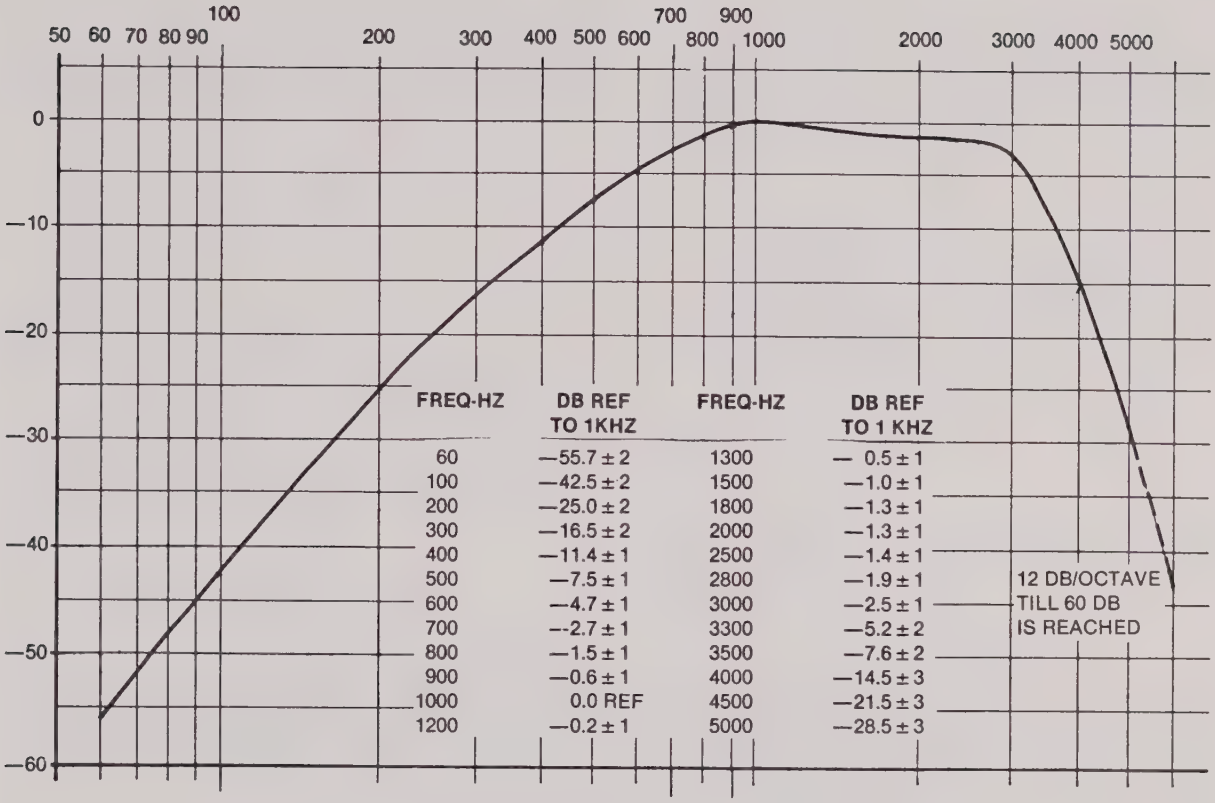
Table 2—1. (Cont'd)

Input Bridging Impedance:	greater than 45 kohms
Noise To Ground Impedance:	greater than 800 kohms between tip and ring greater than 600 kohms between tip and ring shorted together (dc blocked)
POWER	
Battery:	rechargeable gel-type batteries supply approximately 10 hours of continuous use
External:	also operates with 105-125 Vac 47 to 440 Hz
PHYSICAL	
Size:	12 w x 11 h x 17 d inches (30.5 w x 27.9 h x 43.2 d cm)
Weight:	36 lb (16.4 kg)
ENVIRONMENT	
Temperature:	operating: 0°C to 50°C (32°F to 122°F) non-operating: −40°C to 75°C (−40°F to 167°F)
Relative Humidity:	10 to 95%



*EXCLUDING ANY FLAT INSERTION LOSS

Figure 2—1. ERL Filter Response



FREQ-HZ	DB REF TO 1KHZ	FREQ-HZ	DB REF TO 1 KHZ
60	−55.7 ± 2	1300	− 0.5 ± 1
100	−42.5 ± 2	1500	−1.0 ± 1
200	−25.0 ± 2	1800	−1.3 ± 1
300	−16.5 ± 2	2000	−1.3 ± 1
400	−11.4 ± 1	2500	−1.4 ± 1
500	−7.5 ± 1	2800	−1.9 ± 1
600	−4.7 ± 1	3000	−2.5 ± 1
700	−-2.7 ± 1	3300	−5.2 ± 2
800	−1.5 ± 1	3500	−7.6 ± 2
900	−0.6 ± 1	4000	−14.5 ± 3
1000	0.0 REF	4500	−21.5 ± 3
1200	−0.2 ± 1	5000	−28.5 ± 3

Figure 2−2. C-Message Filter Response

SECTION 3

INSTALLATION

3.1 This section contains information necessary for installation and interfacing the Level Tracer. The information includes:

a. initial inspection

b. power/grounding requirements, and

c. interfacing.

3.2 INITIAL INSPECTION

3.3 The Model 8100 Level Tracer was carefully inspected both mechanically and electrically before shipment. It should be free of defects and should be operating correctly when received. To confirm this, the test set should be inspected for damage in transit. If damage has occurred, file a claim with the carrier.

3.4 POWER REQUIREMENTS

3.5 The Level Tracer can be operated from the internal battery pack, or from an external 115 Vac power source. Paragraph 3.6 explains the internal battery characteristics. Paragraph 3.9 explains the ac power characteristics.

3.6 BATTERY POWER

3.7 The internal battey pack consists of two 6-Vdc rechargeable batteries connected in parallel. The battery pack provides 8 to 10 hours of continuous use without need for recharging. Allow the batteries to charge anytime the Level Tracer is not operating on battery power. Frequently charged batteries have a longer lifetime and provide maximum operating time. To recharge the batteries, plug the Level Tracer into an external ac power source, it is not necessary to turn on the Level Tracer. Recharging time for batteries is approximately 10 to 12 hours. The Level Tracer can be operated on ac power source while recharging the batteries.

CAUTION

The batteries must not remain in a discharged or partially discharged condition for more than two days. Chemical reactions within the batteries may reduce battery capacity. A discharged battery stored for an extended period can later fail to accept a charge.

3.8 Batteries **must** be charged for at least 48 hours before extended storage (two weeks or more) regardless of battery charge condition. Preferred storage temperature is 21°C (70°F) or below. Stored batteries must be recharged at least twice per year. Higher temperatures require more frequent charging.

NOTE

If, after a normal recharging period (10 to 12 hours), the Level Tracer operates in battery mode for less than 3 hours then one of the batteries cannot hold a charge. Remove all the batteries and tape the ends of all loose leads. The Level Tracer can still be operated from an ac power source.

3.9 AC POWER

3.10 The Level Tracer can be operated from any power source supplying 105 to 125 Vac, 47 to 440 Hz. Power dissipation is 24 VA maximum.

3.11 GROUNDING REQUIREMENTS

3.12 To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the front panel and cabinet be grounded. The Level Tracer is equipped with a three-conductor power cable which, when plugged into an appropriately grounded receptacle, grounds the instrument.

WARNING

To ensure operator protection, connect the front panel GROUND terminal to earth ground when operating in the battery mode.

3.13 ENVIRONMENTAL REQUIREMENTS

3.14 OPERATING TEMPERATURE

3.15 In order for the Level Tracer to operate within the specifications listed in Table 2−1, the operating temperature must be within the range of 0 to +50°C (+32 to +122°F).

3.16 RELATIVE HUMIDITY

3.17 The relative humidity allowable for proper operation of the Level Tracer is 10 to 95% for temperatures below 40°C (+64°F). As temperatures increase above 40°C, the relative humidity allowable for proper operation will decrease.

3.18 INTERFACE REQUIREMENTS

3.19 The Level Tracer is equipped with input/output connectors. The TIP and RING connectors are standard size binding posts. The binding posts for each TIP/RING pair are spaced to accept a standard dual banana plug.

3.20 PREPARATION FOR USE

3.21 The Level Tracer requires little preparation for use. Place the Level Tracer on a convenient work surface and remove the front cover. The Level Tracer may be used standing on end, or the carrying handle may be locked in position to tilt the Level Tracer at a convenient viewing angle.

SECTION 4

OPERATION

4.1 This section provides the information needed for proper operation of the Level Tracer in a wide variety of applications. The information is organized as follows:

a. Brief descriptions of front panel **controls and indicators** (paragraph 4.2);

b. Procedures for making each of the Level Tracer's **five basic measurements** . . . level, impedance, noise, return loss, frequency . . . (paragraph 4.20);

c. Procedures and information needed for using the five basic measurements in a number of diverse **applications** (paragraph 4.45).

4.2 FRONT PANEL CONTROLS AND INDICATORS

4.3 Figure 4—1 shows the front panel controls and Table 4—1 briefly describes the function of each control. The front panel controls, indicators, switches, and connectors have been divided into functional groups. These functional groups are: (1) power, (2) CRT, (3) display, (4) receive, (5) transmit, and (6) frequency.

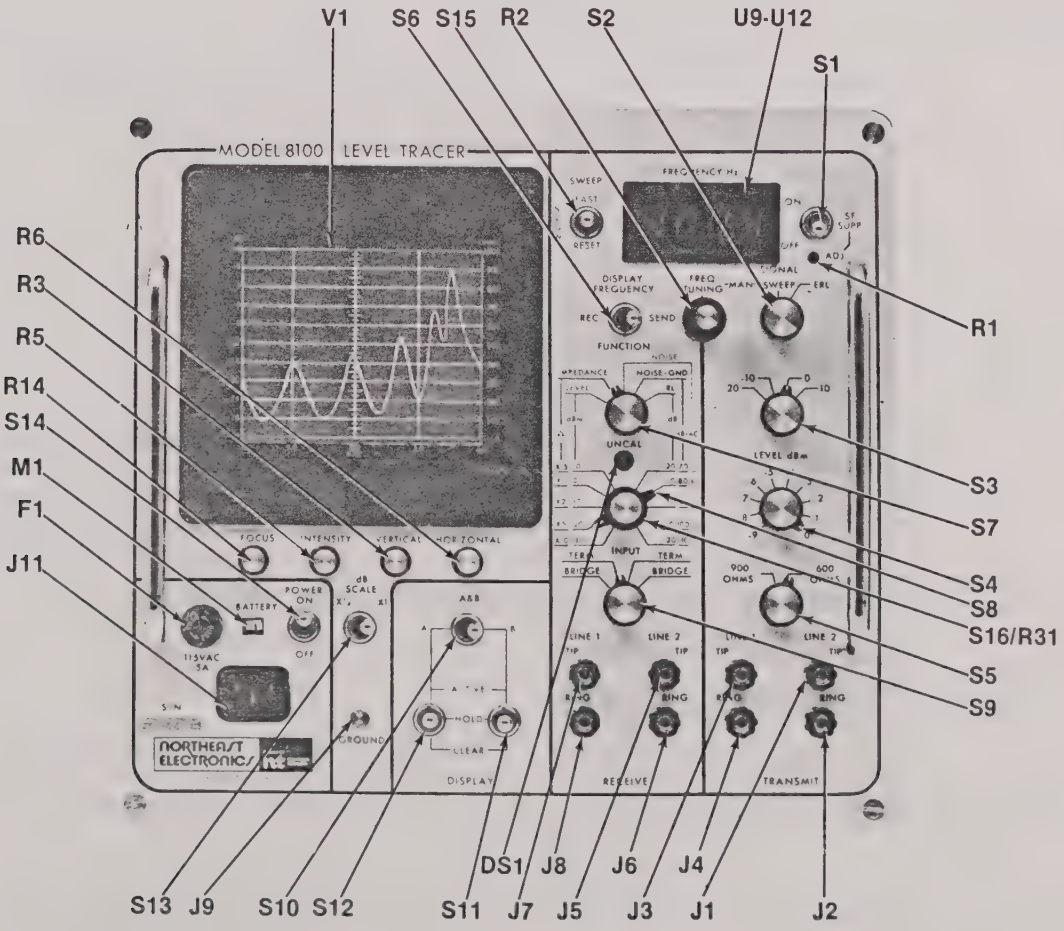


Figure 4—1. Front Panel Controls And Indicators.

Table 4—1. Controls And Indicators.

REF DESIG	CONTROL, INDICATOR OR CONNECTOR	FUNCTION
POWER GROUP		
F1	115 VAC .5A fuse	Protects against excessive current in the input ac line.
M1	BATTERY meter	Monitors capacity of battery. Batteries should be recharged when meter shows low capacity (meter pointer over red zone).
S14	POWER ON/OFF toggle switch	When on, applies power to the unit.
J11	power jack	Connects unit to a power source of 105-125 Vac, 47 to 440 Hz. Recharges batteries whenever connected to a power source regardless of the position of the POWER switch.
CRT GROUP		
R14	FOCUS potentiometer	Provides adjustment to obtain a well-defined trace.
R5	INTENSITY potentiometer	Controls trace brightness.
R3	VERTICAL potentiometer	Controls trace vertical position.
R6	HORIZONTAL potentiometer	Controls trace horizontal position.
S13	dB SCALE switch	Sets the vertical dB scale factor. Switch inoperative when FUNCTION switch is set at IMPEDANCE. Variations on an "active" trace from 2 dB above to 8 dB below the 0 dB reference line are magnified by a factor of 4. A previously recorded ("hold") trace cannot be magnified.
J9	GROUND binding post terminal	For Level Tracer connection to earth ground. **WARNING** **To ensure operator protection, connect the GROUND binding post to earth ground when operating in the battery mode.** NOTE When measuring noise to ground in battery mode, ground reference must be supplied via this terminal to insure correct measurement results.

Table 4—1. (Cont'd)

REF DESIG	CONTROL, INDICATOR OR CONNECTOR	FUNCTION
DISPLAY GROUP		
V1	CRT display cathode ray tube	Displays the contents of the trace memories as controlled by the display group switches.
S10	DISPLAY toggle switch	Determines which trace will be displayed. A - Display shows the content of trace A memory only. The content of a cleared memory appears as a straight line at the "clear" graticule line. A & B - Display shows the contents of trace A and B memories. If both memories are "active" or are "cleared" then a single trace will appear on the display since the contents of the memories are identical after updating. B- Display shows the contents of B memory only. NOTE A trace memory can be updated without being displayed.
S11, S12	Memory Trace A and B toggle switches	Determines the memory state for each trace. ACTIVE - Allows memory to be continuously updated. A trace memory can be updated without being displayed. HOLD - Retains the contents of the memory. The scale factor of a "hold" trace memory is set by the dB SCALE switch at the time updating occurred. CLEAR - Erases content of the memory.
RECEIVE GROUP		
S7	FUNCTION test select rotary switch	Selects the operating mode. LEVEL - Transmits a test signal and/or measures the amplitude of a received test signal. The LEVEL dBm switches set the send level. These switches are inoperative for all other positions of the FUNCTION switch. IMPEDANCE-Transmits a constant current into a circuit under test and mesures the resulting voltage drop. Results give the impedance of the circuit under test. During an impedance measurement, the IMPEDANCE switch has no effect on the test set up.

Table 4—1. (Cont'd)

REF DESIG	CONTROL, INDICATOR OR CONNECTOR	FUNCTION
		NOISE - Measures metallic (balanced) noise with both tip and ring isolated from earth ground. A C-message weighting filter is used for all noise measurements. NOISE/GND - Measures noise level between two sides of a balanced line. The results are true values between 38 dBrnC and 118 dBrnC; no corrections are necessary. NOTE It is necessary to establish a good earth ground or system ground and connect it to the Level Tracer GROUND terminal when making noise to ground measurements. RL - Measures 2-wire return loss of a circuit under test compared with a standard or reference circuit. The test may be manually tuned or automatically swept. For ERL (echo return loss) test, a band-limited noise source is substituted as the test signal via the SIGNAL switch. During 2-wire return loss (RL) measurements the INPUT and IMPEDANCE switches have no effect on the test set up.
S8	FUNCTION range select rotary switch	Establishes the display 0 dB reference line for level, noise, and return loss measurements. Sets the scale factor for impedance measurements.
S16/R31	uncalibrated switch/potentiometer	Reduces the input level by 0 to 9 dB. This control enables the separation of a continuously updated trace and a previously recorded trace. Also useful in 2-wire return loss mode when the trace is driven off screen by noise (as in a split pair).
DS1	UNCAL LED indicator	When lighted, indicates that uncalibrated gain control is engaged.
S9	INPUT rotary switch	Selects the input line to be measured and determines whether to terminate or bridge the line. The INPUT switch has no effect during 2-wire return loss (RL) measurements.
J7/J8	LINE 1 TIP/RING binding posts	Connect the receive section to a line under test.
J5/J6	LINE 2 TIP/RING binding posts	Connect the receive section to a line under test.

Table 4—1. (Cont'd)

REF DESIG	CONTROL, INDICATOR OR CONNECTOR	FUNCTION
TRANSMIT GROUP		
S3/S4	LEVEL dBm −20 to 10 and −9 to 0 rotary switches	The combined settings of the two LEVEL dBm switches set the transmit level when the FUNCTION switch is set at LEVEL.
S5	IMPEDANCE rotary switch	Sets the output impedance and input terminating impedance. Always place the IMPEDANCE switch at the appropriate setting when bridging the line under test. The IMPEDANCE switch has no effect during 2-wire return loss (RL) or impedance measurements.
J3/J4	LINE 1 TIP/RING binding posts	Connect the transmit section to a line under test.
J1/J2	LINE 2 TIP/RING binding posts	Connect the transmit section to a line under test.
FREQUENCY GROUP		
U9/U12	FREQUENCY - Hz 4-digit display	Displays the measured frequency—either the send or receive frequency.
S6	DISPLAY FREQUENCY toggle switch	Selects the send or receive frequency as the measured frequency. The measured frequency also appears on display screen as a frequency marker. A flashing display indicates the measured frequency amplitude is too low to be accurately measured. The frequency counter can count a signal in the presence of noise if the signal-to-noise ratio is greater than 15 dB. The frequency counter locks on the higher level signal of two fixed frequencies separated by at least 100 Hz with a signal-to-signal ratio greater than 5 dB.
S2	SIGNAL rotary switch	Controls the send frequency mode. MAN - Fixed frequency set by FREQ TUNING control SWEEP - Automatic swept frequency from 200 to 4000 Hz. Sweep speed (3 sec/sweep or 6 sec/sweep) set by SWEEP SPEED switch. ERL - Band limited noise signal. Normally used for echo return loss measurements. NOTE The ERL test signal has a fixed output level of −10 dBm during 2-wire return loss (RL) measurements. The ERL test signal output level is controlled by the LEVEL dBm switches in LEVEL mode (4-wire return loss measurements).

Table 4—1. (Cont'd)

REF DESIG	CONTROL, INDICATOR OR CONNECTOR	FUNCTION
S15	SWEEP SPEED toggle switch	Sets the sweep frequency speed when the SIGNAL switch is at SWEEP. Switch is inoperative when SIGNAL switch is set at MAN or ERL. FAST: 3 seconds per sweep SLOW: 6 seconds per sweep RESET: stops the sweep and holds the send frequency below 200 Hz.
R2	FREQ TUNING potentiometer with coarse and fine adjustment knobs	Adjusts the send frequency when the SIGNAL switch is set a MAN. Small knob is the coarse adjust and large knob is the fine adjust.
S1	SF SUPP toggle switch	When set at ON, skips transmission over 300-Hz band set between 2000 Hz and 4000 Hz. The display trace shows the skipped transmission band as a "dropout" in sweep mode. The frequency display shows a jump across the skipped transmission band in manual mode as the frequency is tuned into the skipped band.
R4	SF SUPP ADJ potentiometer, screwdriver adjustment	Adjusts the skip center frequency between 2000 Hz and 4000 Hz. The skip center frequency is factory set at 2600 Hz.

4.4 GENERAL OPERATING INSTRUCTIONS

4.5 PRELIMINARY SET UP

4.6 Applying Power

4.7 The Level Tracer may be powered by an external ac power source or from its own internal battery pack. For battery operation skip steps 1 through 3.

1. Remove power cord from accessory case in the cover.

2. Connect power cord to connector on front panel.

3. Connect power cord to an ac power source (105 to 125 Vac, 47 to 440 Hz).

WARNING

To ensure operator protection, connect the front panel GROUND terminal to earth ground when operating in battery mode.

4. Set POWER switch on.

5. If operating in battery mode, observe that the BATTERY meter pointer is over the white zone indicating sufficient battery capacity. If BATTERY meter pointer is over the red zone then perform steps 1 through 3. (Batteries will be recharged while the Level Tracer is operating from an ac power source.)

6. Observe that the FREQUENCY - Hz display lights up.

4.8 Adjusting The CRT Display

1. Connect the TRANSMIT section LINE 1 TIP and RING binding posts to the RECEIVE section LINE 1 TIP and RING binding posts.

2. Set the Level Tracer switches as follows:

a. dB SCALE at X1

b. DISPLAY at A & B

c. Memory trace A at CLEAR then at ACTIVE

d. Memory trace B at CLEAR then at ACTIVE

e. FUNCTION test select at LEVEL

f. FUNCTION range select at 0 dBm

g. Uncalibrated gain fully counterclockwise (red UNCAL indicator not on)

h. INPUT at LINE 1 TERM

i. SWEEP SPEED at SLOW

j. SIGNAL at SWEEP

k. SF SUPP at OFF

3. Adjust the INTENSITY control to obtain desired trace brightness. The trace will bloom if the intensity is set too high and a sharp trace will not be obtained.

4. Adjust the FOCUS control to obtain a sharp trace.

5. Set the transmit level at 0 dBm (LEVEL dBm switch settings of 0 and 0).

6. Allow the traces to be completely updated. The two traces are superimposed and appear as one straight line.

7. Adjust the VERTICAL position control to place the traces on the 0 dB graticule line.

8. Set the SIGNAL switch at MAN and adjust the FREQ TUNING control to obtain 2000 ± 1 Hz on the FREQUENCY - Hz display.

9. Adjust the HORIZONTAL control to place the frequency marker directly on the 2.0 KHZ vertical graticule line.

NOTE

Steps 10 through 20 are optional. These steps check the trace's vertical and horizontal accuracies.

10. Set the SIGNAL switch at SWEEP.

11. Set the transmit level at +4 dBm (LEVEL dBm switch settings of 10 and −6).

12. Allow trace to be completely updated then set the memory trace A switch at HOLD.

13. Set the transmit level at −28 dBm (LEVEL dBm switch settings of −20 and −8).

14. Allow trace to be completely updated then set the memory trace B switch at HOLD.

15. Adjust the VERTICAL control to place the top trace on the +4 dB graticule line. The bottom trace should be on the −28 dB graticule line.

NOTE

If the separation of the two traces is incorrect, refer to calibration in the maintenance section.

16. Set the SIGNAL switch at MAN.

17. Adjust the FREQ TUNING control to obtain 1000 ± 1 Hz on the FREQUENCY - Hz display.

18. Observe that the markers are directly on the 1.0 KHZ vertical graticule line.

19. Adjust the FREQ TUNING control to obtain 3000 ± 10 Hz on the FREQUENCY - Hz display.

20. Observe that the markers are close to the 3.0 KHZ vertical graticule line.

NOTE

If the trace width is incorrect, refer to calibration in the maintenance section.

4.9 STORING AND DISPLAYING MEASUREMENT RESULTS

4.10 The Level Tracer can only measure one signal at a time, but can store measurement results for two circuits under test. Thus to compare two sets of measurement results it is necessary to first measure, store, and hold the test results of one circuit and then to measure and store the test results of the second circuit.

4.11 Memory trace switches A and B determine into which trace memory the measurement results will be stored. To store these results into a trace memory, set the selected memory trace switch (A or B) at ACTIVE. Setting a memory trace switch at HOLD retains the previously recorded data in that trace memory. To erase the contents of a trace memory, set the memory trace switch at CLEAR.

4.12 DISPLAY A/A & B/B switch selects which trace memory will appear on the CRT screen. In positions A or B, only the content of the selected trace memory appears on the screen. The content of a cleared trace memory is shown as a straight line at the "clear" graticule line. In position A & B the contents of both trace memories are seen on the screen simultaneously. (If both memories are "active" or "cleared" then only a single trace seems to be displayed since both traces are identical after updating and are superimposed on each other.)

4.13 MAKING PERMANENT RECORDS OF DISPLAYED TRACES

4.14 Permanent records of measurement results may be made on the graticule overlays supplied with the Level Tracer. Additional graticule overlays (part number 8100-00-124) can be obtained from Northeast Electronics.

4.15 The overlay is placed against the screen with the frosted side of the overlay on the outside. Each end of the overlay is slipped in between the screen and the graticule cover. The overlay is then flattened out against the screen and the overlay pattern is aligned with the screen graticule.

4.16 A pencil or fine point felt tip pen may be used to copy the traces shown on the screen. After removing the overlay, additional information (such as pertinent Level Tracer switch positions and circuit under test descriptions) may be written on the overlay.

4.17 The overlay can then be placed on a photo copier (Xerox or equivalent) to make permanent paper records. The overlay may then be erased and reused.

4.18 ADJUSTING SINGLE FREQUENCY SUPPRESSION

4.19 The Level Tracer has single frequency suppression (SF SUPP) factory set at 2600-Hz. When single frequency suppression is applied, the Level Tracer skips transmission over a 300-Hz band centered about the set single frequency. The SF SUPP band may be repositioned by a user anywhere between 2000 Hz and 4000 Hz. To adjust the position of the SF SUPP band:

1. Set the POWER switch at ON.

2. Connect the TRANSMIT section LINE 1 jacks to the RECEIVE section LINE 1 jacks (tip to tip and ring to ring).

3. Set the Level Tracer control as follows:

   a. SWEEP SPEED at SLOW

   b. SF SUPP at OFF

   c. SIGNAL at MAN

   d. FUNCTION test select at LEVEL

   e. FUNCTION range select at 0 dBm

   f. INPUT at LINE 1 TERM

   g. DISPLAY at A & B

   h. Memory Trace A and B at CLEAR

   i. dB SCALE at X1

4. Set the Level Tracer transmit level at +4 dBm (LEVEL dBm switch settings of 10 and −6).

5. Adjust FREQ TUNING control to obtain the lower edge frequency of the desired suppression band on the FREQUENCY - Hz display. For example: 2450 Hz for an SF of 2600 Hz.

6. Set memory trace A at ACTIVE.

7. Slowly adjust FREQ TUNING control to obtain the upper edge frequency of the desired suppression band on the FREQUENCY - Hz display. For example: 2750 Hz for an SF of 2600 Hz.

8. Set memory trace A switch at HOLD.

9. Set Level Tracer transmit level at 1 dBm (LEVEL dBm switch settings of 10 and −9).

10. Set SIGNAL switch at SWEEP.

11. Set the SF SUPP switch at ON.

12. Set memory trace B switch at ACTIVE.

13. Allow trace B to be updated. The suppression band appears as a gap (drop-out) in trace B.

NOTE

When adjusting single frequency suppression, periodically clear trace B. Disreguard any pulses within the suppression band display.

14. With an alignment tool, adjust SF SUPP ADJ potentiometer R1 (accessible through the front panel) to center the suppression band of trace B over the 4-dB level of trace A.

4.20 **BASIC MEASUREMENT PROCEDURES**

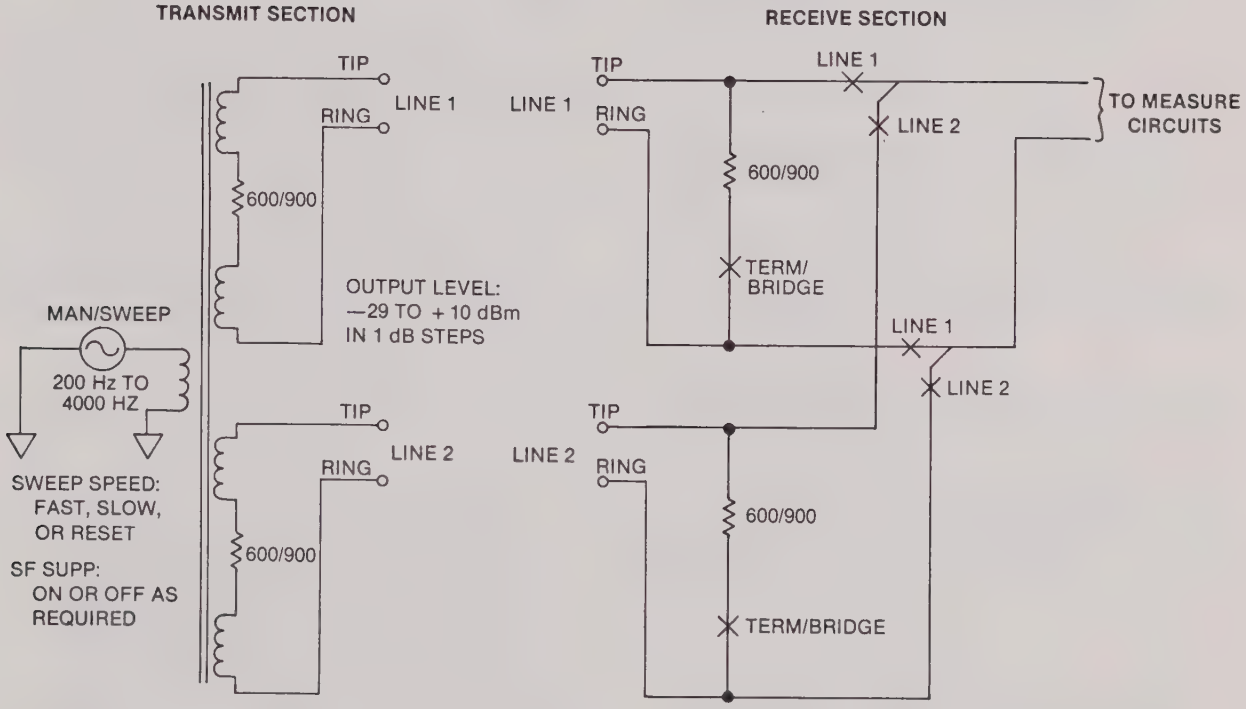
4.21 LEVEL TESTS

4.22 Figure 4−2 shows the Level Tracer's internal configuration with the FUNCTION test select switch at LEVEL. In this configuration the unit can:

a. Transmit a signal into a circuit under test. The signal may be swept (200 Hz to 4000 Hz) or manually tuned and have a level between −29 dBm and +10 dBm into 600 ohms or 900 ohms.

b. Receive a signal from a circuit under test. The incoming signal may be sweeping (200 Hz to 4000 Hz) or fixed tuned. The Level Tracer measure levels between −62 dBm and +18 dBm with a resolution of 0.2 dB. The Level Tracer may bridge or terminate (600 ohms or 900 ohms) the circuit under test.

c. Transmit and receive simultaneously thus permitting loop-around testing.



NOTE:

1. X¼ SCALE SWITCH ONLY AFFECTS THE DISPLAY BUT NOT THE RANGE SELECT SETTING.

RANGE SETTING	MEASUREMENT RANGE (dBm) (X1SCALE)	(X¼ SCALE)
+10	−22 TO +18	+2 TO +12
0	−32 TO +8	−8 TO +2
−10	−42 TO −2	−18 TO −8
−20	−52 TO −12	−28 TO −18
−30	−62 TO −22	−38 TO −28

Figure 4−2. LEVEL Test Configuration

4.23 Transmitting A Level Test Signal

1. If the circuit to be tested uses SF signaling, set the SF SUPP switch at ON.

2. Connect the TRANSMIT section LINE 1 or LINE 2 TIP and RING connectors to the circuit under test.

NOTE

Two circuits under test may be connected to the TRANSMIT section at a time. Each circuit will receive the same level (in dBm) if both circuits have the same characteristic impedance.

3. Set the FUNCTION test select switch at LEVEL.

4. Set the IMPEDANCE switch at the impedance of the circuit under test, either 600 OHMS or 900 OHMS.

5. Set the LEVEL dBm switches at the desired level. The send level is the algebraic sum of the two switch settings. Example: switch settings of 10 and −2 equal a send level of +8 dBm.

6. Set DISPLAY FREQUENCY switch at SEND. The FREQUENCY - Hz display and a frequency marker on the CRT screen both indicate the send frequency.

7. To send a sweeping test signal, set the SIGNAL switch at SWEEP and the SWEEP SPEED switch at either SLOW (6 seconds per sweep) or at FAST (3 seconds per sweep). The RESET setting holds the send frequency below 200 Hz.

NOTE

The FAST speed is useful for quick checks and comparisons on various types of circuits. However, the FAST speed may induce in some circuits a transient phenomena which is not truly representative of actual circuit performance under normal, steady-signal conditions. For such circuits, the SLOW speed must be used to obtain the best, unperturbed traces. The SLOW speed also provides some additional resolution and accuracy.

8. To send a test signal at a fixed frequency, set the SIGNAL switch at MAN and adjust the coarse/fine FREQ TUNING control for the desired send frequency (small knob = coarse, large knob = fine.)

4.24 Receiving/Measuring A Level Test Signal

1. Connect the RECEIVE section LINE 1 or LINE 2 TIP and RING connectors to the circuit under test.

NOTE

Two circuits under test may be connected to the RECEIVE section at a time. The signal from only one circuit under test will be measured by the Level Tracer, as selected by the INPUT switch.

2. Set the FUNCTION test select switch at LEVEL.

3. Set the IMPEDANCE switch at the impedance of the circuit under test, either 600 OHMS or 900 OHMS.

4. Set the INPUT switch at either TERM or BRIDGE (as appropriate) over the LINE 1 lettering to select the circuit under test connected to RECEIVE LINE 1 or over the LINE 2 lettering to select the circuit under test connected to RECEIVE LINE 2.

5. Set the DISPLAY FREQUENCY switch at REC. The frequency of the received signal appears on the FREQUENCY - Hz display and a frequency marker indicates the received frequency on the CRT screen.

NOTE

A fixed-tuned signal appears on the display screen as a pulse at the appropriate frequency position on the screen. The top of the pulse indicates the received level. To obtain a straight line display of a fixed-tuned signal level received from an external source, set the SIGNAL switch at SWEEP and the DISPLAY FREQUENCY switch at SEND.

6. Store the measurement results into a cleared trace memory and display that trace memory (refer to paragraph 4.9).

7. Adjust the FUNCTION range select switch to place the trace as close as possible to the 0 dB reference line. The dB SCALE switch can be set at X1/4 to magnify variations on an "active" trace from 2 dB above to 8 dB below the 0 dB reference line.

NOTE

It may be necessary to clear the trace memory after switching to obtain an accurate trace.

8. The level of the received signal is as follows:
REC LEVEL = (screen reading) X (dB scale factor) + (range select setting).

For example:

a. Screen reading = −6
Scale factor = X1
Range select setting = −20 dBm
Received level = (−6)(1) + (−20) = −26 dBm

b. Screen reading = −16
Scale factor = X1/4
Range select setting = −20 dBm
Received level = (−16)(1/4) + (−20) = −24 dBm

9. To save the contents of a trace memory, set its memory trace switch at HOLD. A second circuit may be tested and its test results stored in the other trace memory.

4.25 **Simultaneously Transmitting And Receiving A Level Test Signal (Loop Around Testing)**

1. If the circuit to be tested uses SF signaling, set the SF SUPP switch at ON.

2. Connect the TRANSMIT section LINE 1 or LINE 2 TIP and RING connectors to the input of the circuit under test.

NOTE

Two circuits under test may be connected to the TRANSMIT section at a time. Each circuit will receive the same level (in dBm) if both circuits have the same characteristic impedance.

3. Connect the RECEIVE section LINE 1 or LINE 2 TIP and RING connectors to the output of the circuit under test.

NOTE

Two circuits under test may be connected to the RECEIVE section at one time. The signal from only one circuit under test will be measured by the Level Tracer as selected by the INPUT switch.

4. Set the FUNCTION test select switch at LEVEL.

5. Set the IMPEDANCE switch at the impedance of the circuit under test, either 600 OHMS or 900 OHMS.

6. Set INPUT switch at either TERM or BRIDGE (as appropriate) over the LINE 1 lettering to select the circuit under test connected to RECEIVE LINE 1 or over the LINE 2 lettering to select the circuit under test connected to RECEIVE LINE 2.

7. Set the LEVEL dBm switches at the desired level. The send level is the algebraic sum of the two switch settings. Example: switch settings of 10 and −5 equal a send level of +5 dBm.

8. Set the DISPLAY FREQUENCY switch at SEND. The FREQUENCY - Hz display and the frequency marker on the CRT screen both indicate the send frequency.

9. To send a sweeping test signal, set the SIGNAL switch at SWEEP and the SWEEP SPEED switch at either SLOW (6 seconds per sweep) or at FAST (3 seconds per sweep). The RESET setting holds the send frequency below 200 Hz.

10. To send a test signal at a fixed frequency, set the SIGNAL switch at MAN and adjust the coarse/fine FREQ TUNING control for the desired send frequency (small knob = coarse, large knob = fine).

11. To send an ERL test signal (for a 4-wire echo return loss measurement) set the SIGNAL switch at ERL.

12. Store the measurement results into a cleared trace memory and display that trace memory (refer to paragraph 4.9).

13. Adjust the FUNCTION range select switch to place the trace as close as possible to the 0 dB reference line. The dB SCALE switch can be set at X1/4 to magnify variations on an "active" trace from 2 dB above to 8 dB below the 0 dB reference line.

14. The level of the received signal is as follows:

REC LEVEL = (screen reading) X (db scale factor) + (range select setting).

For example:

Screen reading = −12
Scale factor = X1
Range select setting = −10 dBm
Received level = (−12)(1) + (−10) = −22 dBm

15. The loss of the circuit under test is the algebraic difference between the send and the received levels (loss = send level − received level). A negative loss shows that the circuit under test has a net gain.

For example:

Send level = −10 dBm
Received level = −27 dBm
Loss = (−10) − (−27) = 17 dB

16. Set the DISPLAY FREQUENCY switch at REC. The frequency of the received signal appears on the FREQUENCY - Hz display. The frequency marker on the CRT screen also shows the received frequency. A fixed-tuned test signal appears on the display screen as a pulse. An ERL test signal appears as a straight line on the display screen.

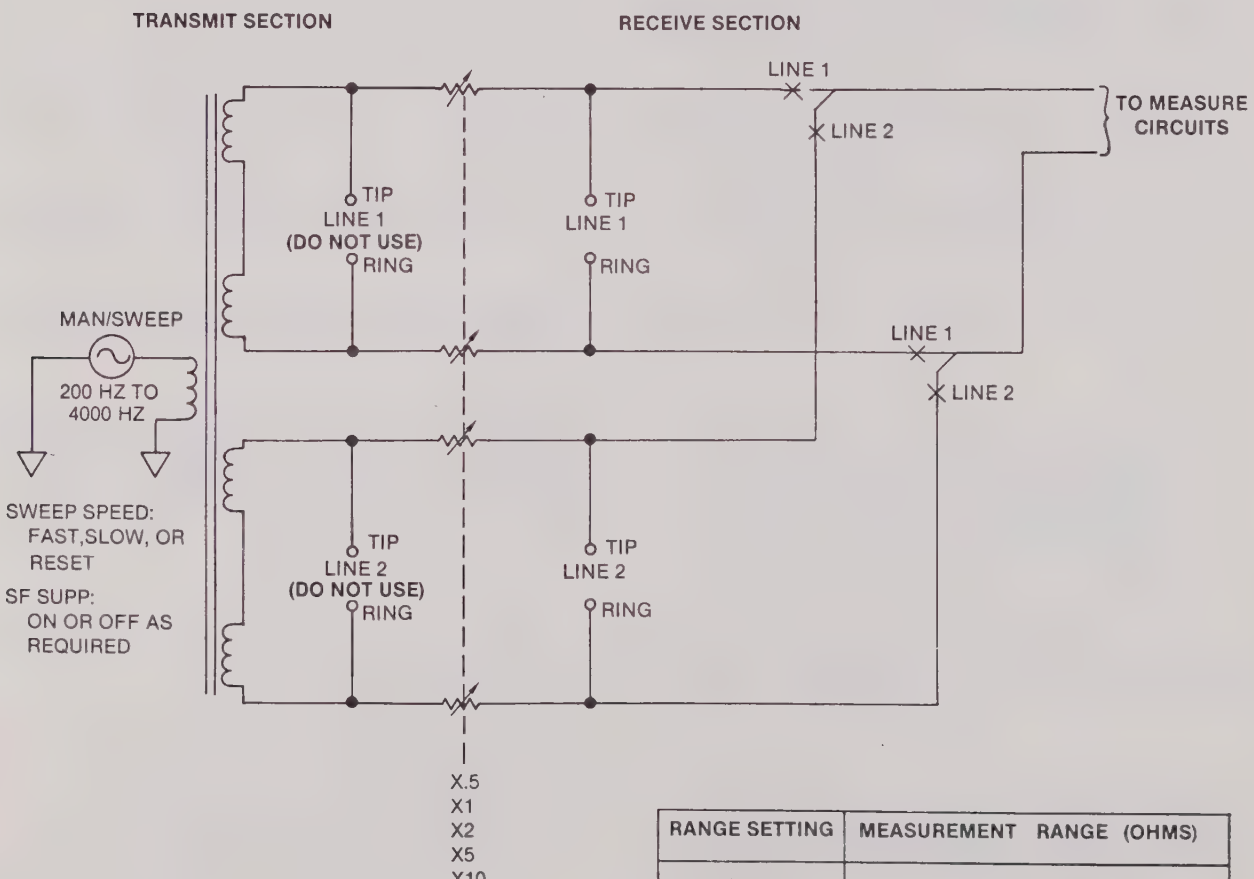
17. To save the content of a trace memory, set its memory trace switch at HOLD. A second circuit may be tested and its test results stored in the other trace memory.

4.26 IMPEDANCE TESTS

4.27 Figure 4—3 shows the Level Tracer's internal configuration with the FUNCTION switch set at IMPEDANCE. In this configuration the unit:

a. Transmits a constant current into a circuit under test.

b. Measures the resulting voltage drop across the circuit under test. The test result gives the magnitude (in ohms) of impedance for the circuit under test.



RANGE SETTING	MEASUREMENT RANGE (OHMS)
X.5	0 TO 500
X1	0 TO 1000
X2	0 TO 2000
X5	0 TO 5000
X10	0 TO 10000

NOTE:

1. DO NOT CONNECT CIRCUIT UNDER TEST TO TRANSMIT LINE 1 OR LINE 2 TIP/RING CONNECTORS

Figure 4—3. Impedance Test Configuration

4.28 The test signal may be swept (200 Hz to 4000 Hz) or manually tuned at a fixed frequency. This allows impedance to be measured at a fixed frequency or as a function of frequency. The Level Tracer can measure impedance up to 10 kohms.

4.29 To measure impedance, perform the following steps.

1. If the circuit to be tested uses SF signaling, set the SF SUPP switch at ON.

2. Connect the RECEIVE section LINE 1 or LINE 2 TIP and RING connectors across the circuit under test (do not use the TRANSMIT connectors).

NOTE

Two circuits under test may be connected to the RECEIVE section at a time. Each circuit will receive the same test signal, but the impedance of only one circuit under test will be measured by the Level Tracer as selected by the INPUT switch.

3. Set the FUNCTION test select switch at IMPEDANCE.

4. Set the INPUT switch at either TERM or BRIDGE position over the LINE 1 lettering to select the circuit under test connected to RECEIVE LINE 1 or over the LINE 2 lettering to select the circuit under test connected to RECEIVE LINE 2.

5. Set DISPLAY FREQUENCY switch at SEND. The test frequency appears on the FREQUENCY - Hz display. A frequency marker on the CRT screen also shows the test frequency.

6. To use a sweeping test signal, set the SIGNAL switch at SWEEP and the SWEEP SPEED switch at either SLOW (6 seconds per sweep) or at FAST (3 seconds per sweep). The RESET setting holds the test frequency below 200 Hz.

7. To use a test signal at a fixed frequency, set the SIGNAL switch at MAN and adjust the coarse/fine FREQ TUNING control for the desired test frequency.

8. Store the measurement results into a cleared trace memory (refer to paragraph 4.9).

9. Adjust the FUNCTION range select switch to obtain the largest display below full scale.

10. The impedance of the circuit under test is as follows:

IMPEDANCE = (screen reading) X (range select setting)

For example:

Screen reading = 700 OHMS
Range select setting = X5
Impedance = (700) X (5) = 3500 ohms

11. To save the content of a trace memory, set its memory trace switch at HOLD. A second circuit may be tested and its test results stored in the other trace memory.

4.30 NOISE TESTS

4.31 Figures 4—4 and 4—5 show the Level Tracer's internal configurations with the FUNCTION switch set at NOISE and NOISE/GND respectively. In NOISE mode, the unit measures the metallic (balanced) noise with both the tip and ring isolated from earth ground. In NOISE/GND mode, the unit measures the noise level between two sides of a line and ground. A C-message weighting filter is used for both NOISE and NOISE/GND measurements.

4.32 **Measuring Metallic Noise**

1. Connect the RECEIVE section LINE 1 or LINE 2 TIP and RING connectors to the near end of the circuit under test.

NOTE

Two circuits under test may be connected to the RECEIVE section at a time. The noise from only one circuit under test will be measured by the Level Tracer as selected by the INPUT switch.

2. Connect a quiet termination (600 or 900 ohms in series with 2.16 uF) at the far end of the circuit under test.

3. Set the FUNCTION test select switch at NOISE.

4. Set the IMPEDANCE switch at the impedance of the circuit under test, either 600 or 900 OHMS.

5. Set the INPUT switch at either TERM or BRIDGE (as appropriate) over the LINE 1 lettering to select the circuit under test connected to RECEIVE LINE 1 or over the LINE 2 lettering to select the circuit under test connected to RECEIVE LINE 2.

6. Store the measurement results into a cleared trace memory (refer to paragraph 4.9).

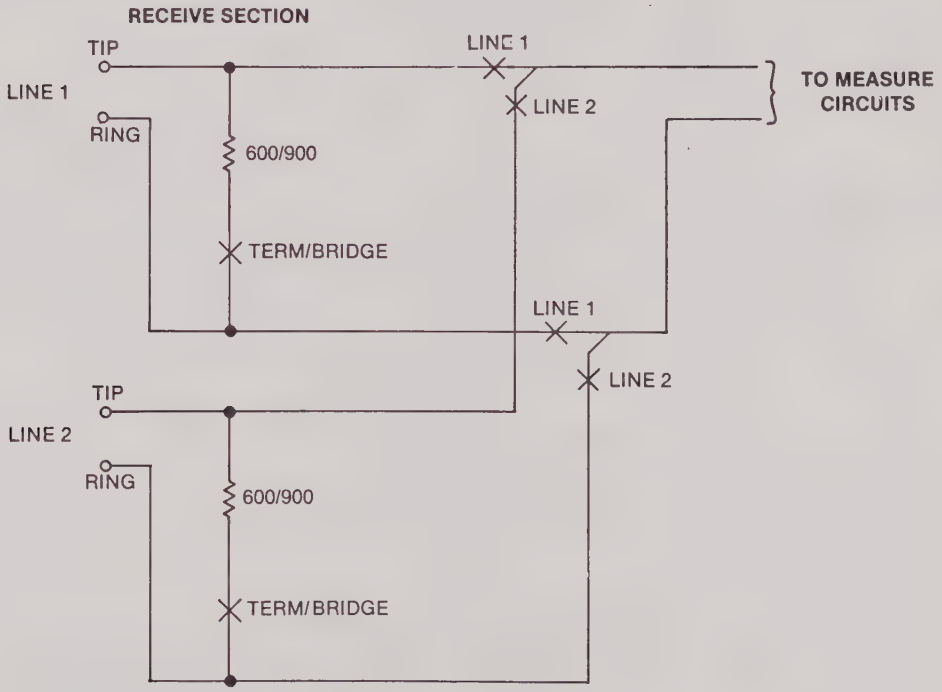
7. Adjust the FUNCTION range select switch to place the trace as close as possible to the 0 dB reference line. The dB SCALE switch can be set at X1/4 to magnify variations on an "active" trace from 2 dB above to 8 dB below the 0 dB reference line.

8. The noise amplitude is as follows:

NOISE = (screen reading) X (dB scale factor) + (range select setting).

For example:

Screen reading = −5
Scale factor = X1
Range select setting = 40 dBrnC
Metallic noise = (−5)(1) + 40 = 35 dBrnC



RANGE SETTING	MEASUREMENT RANGE (dBrnC) (X1 SCALE)	(X¼ SCALE)
30	−2 TO 38	22 TO 32
40	8 TO 48	32 TO 42
50	18 TO 58	42 TO 52
60	28 TO 68	52 TO 62
70	38 TO 78	62 TO 72

NOTE:

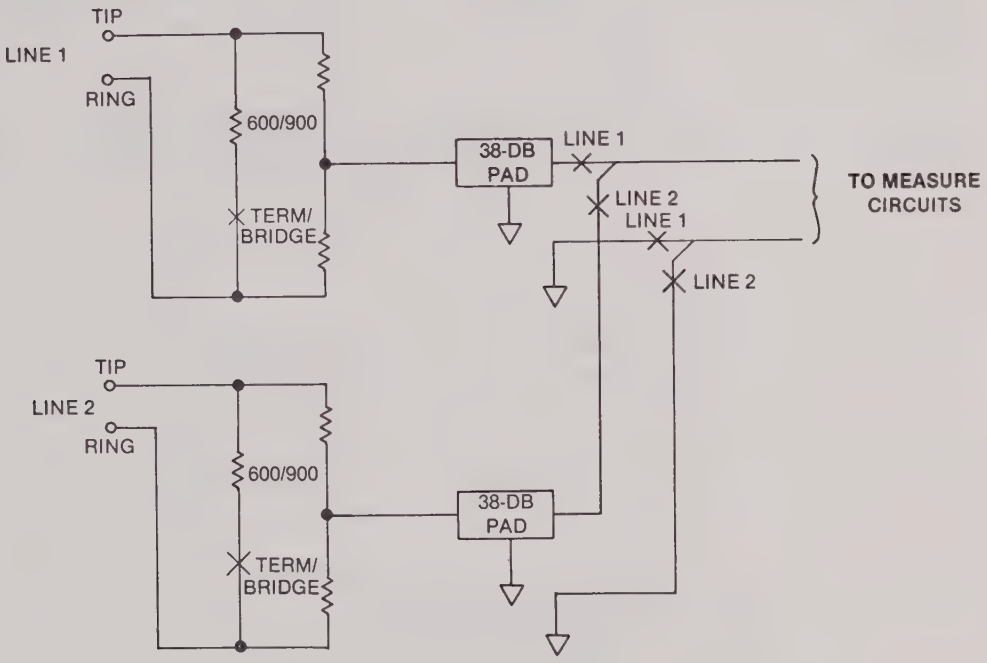
1. TRANSMIT SECTION TERMINATED INTO CHARACTERISTIC IMPEDANCE AND OUTPUT LEVEL REDUCED TO ZERO VOLTS BUT TRANSMIT SECTION SHOULD NOT BE USED AS A QUIET TERMINATION.

2. X¼ SCALE SWITCH ONLY AFFECTS THE DISPLAY BUT NOT THE RANGE SETTING.

Figure 4—4. Metallic NOISE Test Configuration

9. Set the DISPLAY FREQUENCY switch at REC. A steady FREQUENCY - Hz display indicates the presence of a predominant single tone within the noise (60-Hz hum or 1004-Hz holding tone, for example) with a 15 dB signal-to-noise ratio or greater.

10. To save the content of a trace memory, set its memory trace switch at HOLD. A second circuit may be tested and its test results stored in the other trace memory.



RANGE SETTING	MEASUREMENT (X1 SCALE)	RANGE (dBrnC) (X¼ SCALE)
70	38 TO 78	62 TO 72
80	48 TO 88	72 TO 82
90	58 TO 98	82 TO 92
100	68 TO 108	92 TO 102
110	78 TO 118	102 TO 112

NOTE:

1. TRANSMIT SECTION TERMINATED INTO CHARACTERISTIC IMPEDANCE AND OUTPUT LEVEL REDUCED TO ZERO VOLTS BUT TRANSMIT SECTION SHOULD NOT BE USED AS QUIET TERMINATION.

2. X¼ SCALE SWITCH AFFECTS ONLY THE DISPLAY BUT NOT THE RANGE SELECT SETTING.

Figure 4—5. NOISE/GND Test Configuration

4.33 **Measuring Noise To Ground**

1. Connect the RECEIVE section LINE 1 or LINE 2 TIP and RING connectors to the near end of the circuit under test.

NOTE

Two circuits under test may be connected to the RECEIVE section at one time. The noise from only one circuit under test will be measured by the Level Tracer, as selected by the INPUT switch.

2. Connect a quiet termination (600 or 900 ohms in series with 2.16 uF) at the far end of the circuit under test.

NOTE

It is necessary to establish a good earth ground or system ground and connect it to the Level Tracer GROUND terminal when making noise to ground measurements.

3. Ensure that the Level tracer is properly grounded.

4. Set the FUNCTION test select switch at NOISE/GND.

5. Set the IMPEDANCE switch at the impedance of the circuit under test, either 600 OHMS or 900 OHMS.

6. Set the INPUT switch at either TERM or BRIDGE (as appropriate) over the LINE 1 lettering to select the circuit under test connected to RECEIVE LINE 1 or over the LINE 2 lettering to select the circuit under test connected to RECEIVE LINE 2.

7. Store the measurement results into a cleared trace memory and display that trace memory (refer to paragraph 4.9).

8. Adjust the FUNCTION range select switch to place the trace as close as possible to the 0 dB reference line. The dB SCALE switch can be set at X1/4 to magnify variations on an "active" trace from 2 dB above to 8 dB below the 0 dB reference line.

9. The noise-to-ground amplitude is as follows:

NOISE TO GROUND = (screen reading) X (scale factor) + (range select setting).

NOTE

Noise-to-ground test results are true values. No correction is required.

For example:

Screen reading = −20
Scale factor = X1/4
Range select setting = 70 dBrnC
Noise to ground = (−20)(1/4) + 70 = 65 dBrnC

10. Set the DISPLAY FREQUENCY switch at REC. A steady FREQUENCY - Hz display indicates that a predominant tone is present within the noise (60-Hz hum or 1004-Hz holding tone, for example) with a 15 dB signal-to-noise ratio.

11. To save the content of a trace memory, set its memory trace switch at HOLD. A second circuit can be tested and its test results stored in the other trace memory.

4.34 TWO-WIRE RETURN LOSS TESTS

4.35 Figure 4−6 shows the Level Tracer's internal configuration with the FUNCTION switch set at RL. In this configuration the unit is configured as a bridge measurement device to measure the return loss of a circuit compared with a standard or reference circuit. The test signal may be manually tuned or automatically swept. A band limited noise source is substituted as the test signal during echo return loss (ERL) tests.

4.36 To measure return loss (or echo return loss), perform the following steps.

1. If the circuit to be tested uses SF signaling, set the SF SUPP switch at ON.

2. Connect the RECEIVE section LINE 1 (or LINE 2) TIP and RING connectors to a reference circuit or standard.

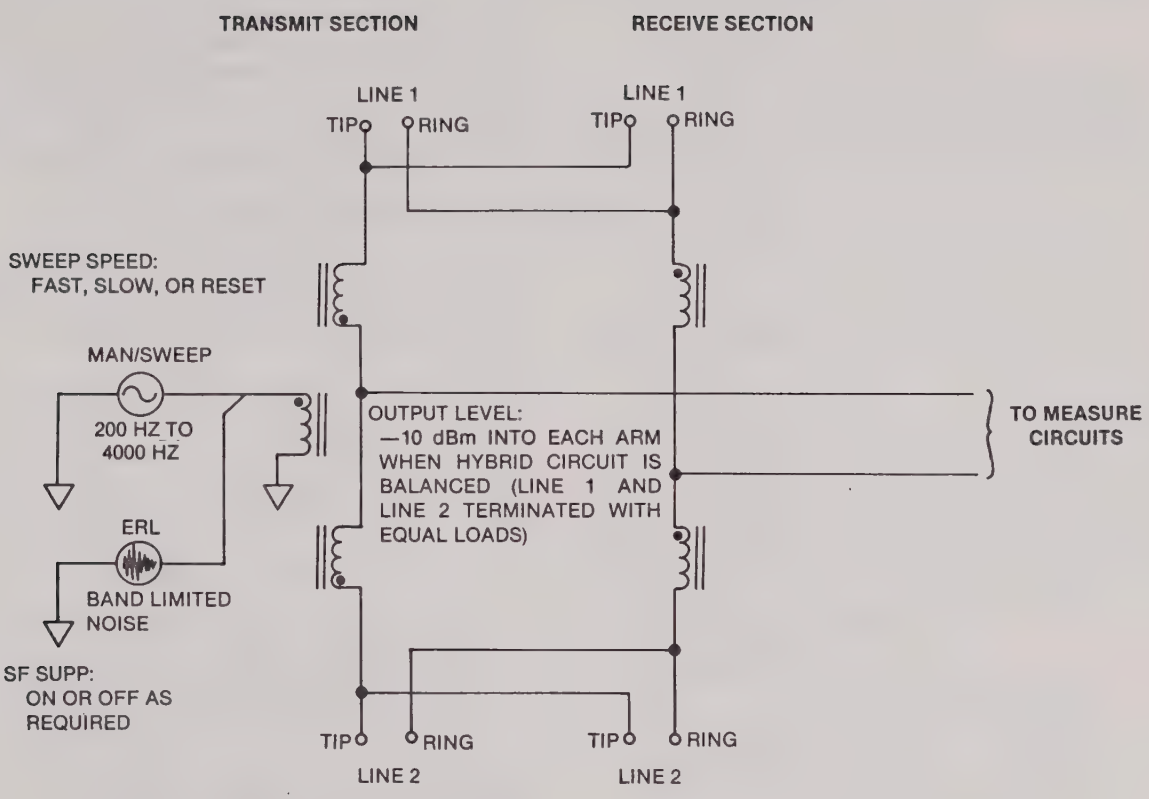
3. Connect the RECEIVE section LINE 2 (or LINE 1) TIP and RING connectors to the circuit under test.

NOTE

Connections to RECEIVE LINE 1 may be interchanged with connections made to RECEIVE LINE 2. The TRANSMIT LINE 1 and LINE 2 connectors permit additional components (for example: buildout capacitor, or compromise network) to be placed across the circuit under test and/or across the standard circuit.

4. Set the FUNCTION test select switch at LEVEL.

5. Set DISPLAY FREQUENCY switch at SEND. The FREQUENCY - Hz display and the frequency marker on the CRT screen show the test frequency.



RANGE SETTING	MEASUREMENT RANGE (dB) (X1 SCALE)	(X¼ SCALE)
—20	12 TO 52	18 TO 28
—10	2 TO 42	8 TO 18
0	0 TO 32	0 TO 8
+10	0 TO 22	——
+20	0 TO 12	——

NOTE:

1. X ¼ SCALE SWITCH AFFECTS ONLY THE DISPLAY BUT NOT THE RANGE SELECT SETTING.

Figure 4—6. Return Loss (RL) Test Configuration

6. To test with a fixed frequency signal, set the SIGNAL switch at MAN and adjust the coarse/fine FREQ TUNING control for the desired test frequency.

7. To test with a sweeping signal, set the SIGNAL switch at SWEEP and the SWEEP SPEED at SLOW (6 seconds per sweep) or at FAST (3 seconds per sweep). The RESET setting holds the test frequency below 200 Hz.

8. To test with a noise signal (for ERL tests), set the SIGNAL switch at ERL.

9. Store the measurement results into a cleared trace memory and display that trace memory (refer to paragraph 4.9).

10. Adjust the FUNCTION range select switch to place the trace as close as possible to the 0 dB reference line. The dB SCALE switch can be set at X1/4 to magnify variation on an "active" trace from 2 dB above to 8 dB below the 0 dB reference line.

11. The return loss is as follows:

RL = −[(screen reading) X (dB scale factor) + (range select setting)].

For example:

Screen reading	=	−20
Scale factor	=	X1
Range select setting	=	−20 dB
RL	=	−[(−20)(1) + (−20)] = 40 dB

12. To save the content of a trace memory, set its memory trace switch at HOLD. A second circuit can be tested and its test results stored in the other trace memory.

4.37 FREQUENCY MEASUREMENTS

4.38 The Level Tracer's frequency counter may be used to:

a. Measure the received frequency of a signal (use level measure mode);

b. Measure the send frequency in level measure mode, the test frequency in impedance measure mode or in return loss measure mode.

c. Determine the value of a transmission parameter (level, impedance, or return loss), at a particular frequency.

4.39 Receive Frequency Measurements

4.40 Fixed-tuned signals with frequencies up to 10 kHz may be measured by the Level Tracer with an accuracy of ± 1 Hz. To measure the frequency of a signal being received, perform a level measurement as described in paragraph 4.24 and observe the FREQUENCY - Hz display with the DISPLAY FREQUENCY switch set at REC.

4.41 Send Frequency Measurements

4.42 The Level Tracer can send a fixed-tuned signal, a swept signal, or an ERL weighted noise signal into a circuit under test. To measure the frequency of a fixed-tuned test signal:

1. Transmit a fixed-tuned signal as described in paragraphs 4.23, 4.25, 4.26, or 4.34.

2. Observe the FREQUENCY - Hz display with the DISPLAY FREQUENCY switch set at SEND.

NOTE

For loop around tests, impedance tests, or two-wire return loss tests the DISPLAY FREQUENCY switch could also be set at REC but the receive frequency might be too weak for accurate frequency measurement.

3. Adjust the coarse and fine FREQ TUNING controls as required to obtain the desired frequency.

4.43 Frequency Marking On The CRT Screen

4.44 The value of a transmission parameter at a specific frequency can be easily determined with the Level Tracer. Perform the following steps.

1. Store, display, and hold a frequency-dependent measurement such as level, impedance or return loss. (Measurements with an ERL signal are frequency independent.)

2. Set the SIGNAL switch at MAN and the DISPLAY FREQUENCY switch at SEND.

3. Adjust the coarse and fine FREQ TUNING controls for the desired frequency.

4. On the CRT display, read the value of the measured parameter highlighted by the frequency marker.

4.45 MEASUREMENT APPLICATIONS

4.46 The Level Tracer's five basic measurements may be used in a variety of different applications. For example, a basic impedance or return loss measurement can be used to determine capacitance and/or resistance.

And, capacitance/resistance determinations can be used to find length of cable to an open or short circuit fault.

4.47 The following paragraphs provide procedures and general information needed for use of the Level Tracer in such applications as:

a. Four-wire echo path loss measurements;

b. Attenuation distortion (gain slope) measurements;

c. Resistance measurements;

d. Capacitance measurements;

e. Cable length measurements;

f. Frequency shift measurements;

g. Circuit balance measurements;

h. Through balancing procedures;

i. Terminal balancing procedures;

j. Structural return loss measurements;

k. Impedance compensator adjustments;

l. Fault location on cables.

4.48 FOUR-WIRE ECHO PATH LOSS MEASUREMENT

4.49 The level measurement capability of the Level Tracer can be used to measure the echo path loss on a 4-wire trunk. This echo path loss equals twice the one-way trunk loss plus the transhybrid loss at the far end.

4.50 Perform the following steps.

1. Connect the transmit pair of the 4-wire trunk under test to the Level Tracer's TRANSMIT section LINE 1 (or LINE 2) TIP and RING connectors.

2. Connect the receive pair of the 4-wire trunk under test to the RECEIVE section LINE 1 (or LINE 2) TIP and RING connectors.

3. Ensure that the distant end of the circuit under test has a quiet termination.

4. Perform a level test (refer to paragraph 4.21.) The ERL signal may be used as a test signal.

5. The echo path loss equals the algebraic difference between the send and receive levels.

ECHO PATH LOSS = (send level) − (receive level)

For example:

Send level = 0 dBm
Receive level = −43 dBm
Echo path loss = (0) − (−43) = 43 dB

6. The return loss of the 4-wire circuit is equal to the echo path loss adjusted for any difference in the expected transmission levels (TLPs) of the sending and receiving sides due to amplifications, pads, or transhybrid loss.

4.51 ATTENUATION DISTORTION (GAIN-SLOPE) MEASUREMENT

4.52 Attenuation distortion is a difference in transmission loss at one frequency with respect to the loss at another frequency. Thus, attenuation distortion gives a numerical measure of a circuit's frequency response.

4.53 Attenuation distortion is typically found by comparing a circuit's loss at 404 Hz and 2804 Hz with the same circuit's loss at 1004 Hz. The differential values resulting from the comparisons are called the slopes at 404 Hz and 2804 Hz.

4.54 The Level Tracer is well suited for these measurements since the display gives the circuit's frequency response and manual tuning can be used to mark the frequencies of interest on the response curve.

4.55 Perform the following steps.

1. Store, display, and hold the frequency response curve of the circuit under test using the level loop around test (refer to paragraph 4.25).

NOTE

Test signals for attenuation distortion measurements are typically transmitted into a circuit at −13 to −16 dBm. Specific levels and test frequencies to be used in different applications are specified by the applicable practice.

2. Manually tune the send frequency to 404 Hz, 1004 Hz, and 2804 Hz. Record the level received at each of these frequencies.

3. The Level Tracer output level is constant as its sweeps and therefore the losses at 404 Hz, 1004 Hz, and 2804 Hz need not be separately calculated. The slopes are obtained directly from the following simple formulas:

Slope (404) = Rec Level (1004) − Rec Level (404)
Slope (2804) = Rec Level (1004) − Rec Level (2804)

A higher loss (lower received level) at 404 Hz (or 2804 Hz) than at 1004 Hz produces a positive slope value.

NOTE

An alternate method is to position the 1004 Hz point of the response curve on the 0 dB reference line (using the LEVEL dBm, FUNCTION range select, and UNCAL switches). The slopes at 404 Hz and 2804 Hz can be read directly on the display screen disregarding the LEVEL dBm and FUNCTION range select switch settings. Recall that a negative reading at 404 Hz or 2804 Hz represents a positive slope value.

4.56 RESISTANCE MEASUREMENT

4.57 Either one of two methods may be used to measure resistance with the Level Tracer. The first method is a straight-forward impedance test. In the second method a return loss test compares the unknown resistance with a variable reference resistance. The first method is quicker, but the second method is more accurate.

4.58 **Resistance Measurement, Impedance Method**

1. Store, display, and hold the impedance curve of the unknown resistance (refer to paragraph 4.26) with a sweep frequency test signal. Set the FUNCTION range select switch to obtain a trace as close to the center of the display as possible.

2. Read the resistance off the screen and multiply the reading by the ohms scale factor.

4.59 **Resistance Measurement, Return Loss Method**

1. Connect the unknown resistance and a known resistance (use a precision resistance substitution box) to the RECEIVE section LINE 1 and LINE 2 connectors respectively. Perform a return loss measurement (refer to paragraph 4.34).

2. Substitute known resistance values until a maximum return loss is obtained. A return loss of 33 dB or greater indicates that the unknown resistance is within ±5% of the reference resistance. If the return loss exceeds 46 dB then the unknown and the reference resistances are within 1% of each other. Refer to Table 4–2.

NOTE

The trace moves downward (increasing return loss) as the reference resistance approaches the unknown resistance. A change from a downward motion to an upward motion indicates that the reference resistance value has passed the unknown resistance value (either from a higher value to a lower value or from a lower value to a higher value).

4.60 CAPACITANCE MEASUREMENT

4.61 Three methods are available for measuring capacitance with the Level Tracer. The first method consists of an impedance test to obtain the reactance of the unknown capacitance at a specific frequency. The measured reactance is then converted into its equivalent capacitance with the aid of a chart. The second method uses the impedance test to obtain the reactance curves of an unknown capacitance and a reference capacitance. The reference capacitance is changed until two matching reactance curves are obtained, at which point the reference capacitance equals the unknown capacitance. In the third method, a return loss test compares the unknown capacitance with a variable reference capacitance. Different values of reference capacitance are used until a maximum return loss is obtained.

4.62 The first two methods are quicker than the third method, but the third method is more accurate. In addition, the third method can measure a wider range of capacitance values than either the first or second method. The first method has a narrower measurement range than the second method, but does not require any reference capacitance.

NOTE

The basic measurements used in theses three methods are suitable for testing **capacitors only** and should not be used on circuits containing inductance or resistance . . . such as loaded and/or terminated cables. Procedures for measuring capacitance on cables are given in paragraph 4.66 under "CABLE LENGTH MEASUREMENTS".

Table 4—2. Return Loss/Percentage Difference Relationship

MEASURED RETURN LOSS (dB)	% DIFFERENCE BETWEEN MEASURED COMPONENT AND REFERENCE COMPONENT
52	−0.50 to + 0.50
51	−0.56 to + 0.57
50	−0.63 to + 0.63
49	−0.71 to + 0.71
48	−0.79 to + 0.80
47	−0.89 to + 0.90
46	−1.00 to + 1.01
45	−1.12 to + 1.13
44	−1.25 to + 1.27
43	−1.41 to + 1.43
42	−1.58 to + 1.60
41	−1.77 to + 1.80
40	−1.98 to + 2.02
39	−2.22 to + 2.27
38	−2.49 to + 2.55
37	−2.79 to + 2.87
36	−3.12 to + 3.22
35	−3.49 to + 3.62
34	−3.91 to + 4.07
33	−4.38 to + 4.58
32	−4.90 to + 5.15
31	−5.48 to + 5.80
30	−6.13 to + 6.53
29	−6.85 to + 7.36
28	−7.66 to + 8.29
27	−8.55 to + 9.35
26	−9.55 to +10.55

4.63 Capacitance Measurement, Reactance Conversion Chart Method

1. Store, display, and hold the reactance curve of the unknown capacitance using the impedance test (refer to paragraph 4.26) with a sweep frequency test signal. Set the FUNCTION range select switch to obtain a reactance curve which occupies most of the display screen.

2. Manually tune the send frequency at one of the following listed frequencies to obtain a well-defined frequency marker somewhere near the center of the display screen.

a. 3979 Hz
b. 3183 Hz
c. 2653 Hz
d. 2274 Hz
e. 1989 Hz
f. 1768 Hz
g. 1592 Hz
h. 1061 Hz
i. 796 Hz
j. 531 Hz
k. 398 Hz
l. 318 Hz
m. 265 Hz
n. 227 Hz

3. Use Figure 4—7 to convert the measured reactance into its equivalent capacitance for the test signal frequency used.

a. Find the intersection point of the measured reactance and the frequency used.

b. Move vertically up to read the capacitance value.

For example:

(1) Test signal frequency = 1592 Hz
Measured reactance = 1500 ohms
Read 0.068 uF off curve G

(2) Test signal frequency = 1989 Hz
Measured reactance = 1000 ohms
Read 0.08 uF off curve D

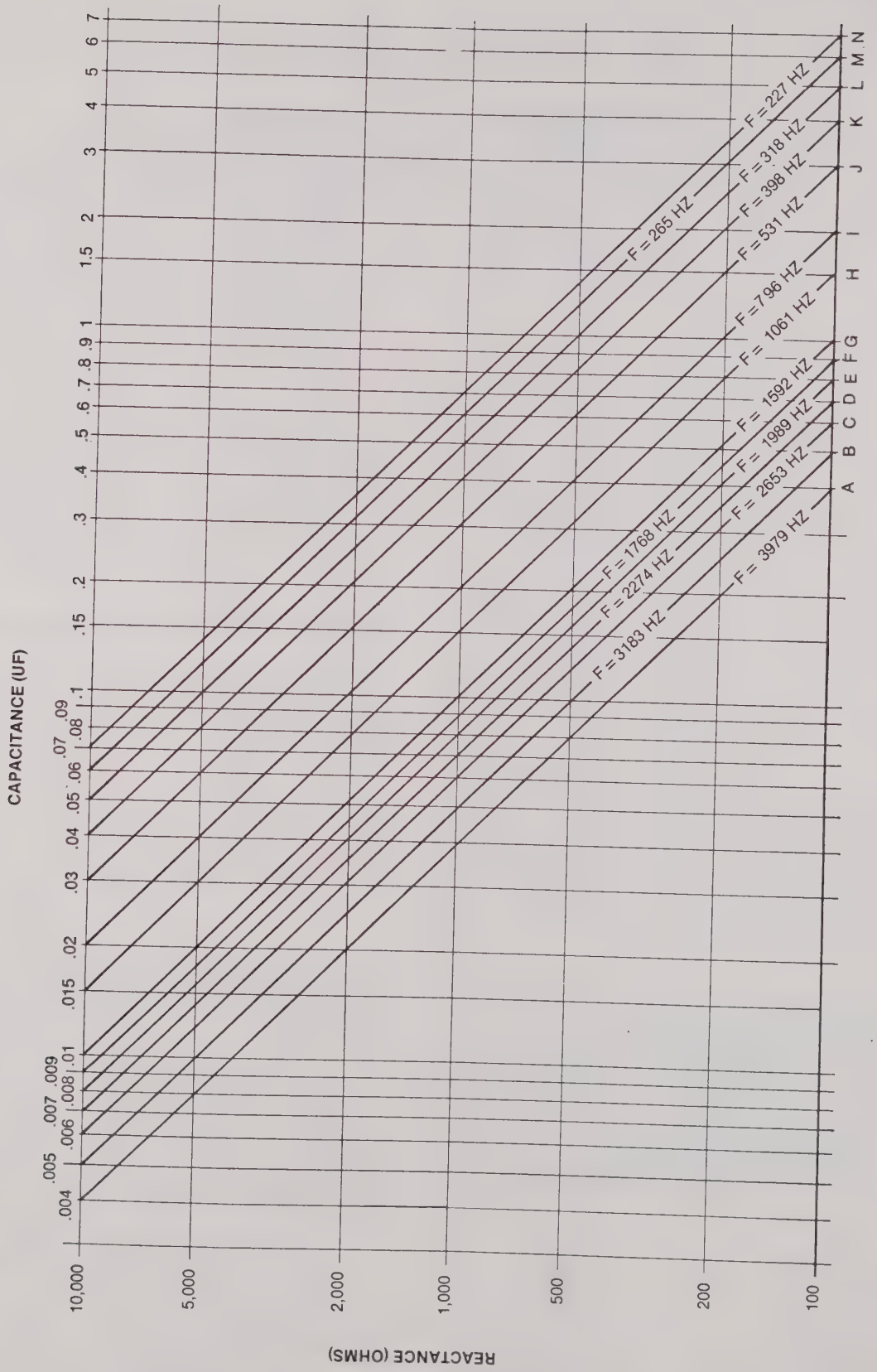


Figure 4—7. Reactance To Capacitance Conversion Chart

4.64 Capacitance Measurement, Impedance Comparison Method

1. Store, display, and hold the reactance curve of the unknown capacitance using the impedance test (refer to paragraph 4.26) with a sweep frequency test signal. Set the range select switch to obtain a reactance curve which occupies most of the display screen.

2. Store and display on the other trace memory the reactance curve of a known capacitance (a capacitance substitution box may be used). Substitute known capacitance values until the two traces are superimposed on each other. The known capacitance now equals the unknown capacitance. All Level Tracer controls must remain at the same settings used in step 1 except that the uncalibrated gain control may be used to separate the two traces when the traces are very close to each other.

4.65 Capacitance Measurement, Return Loss Method

1. Connect the unknown capacitance and a known capacitance (use a precision capacitance substitution box) to the RECEIVE section LINE 1 and LINE 2 connectors respectively. Perform a return loss measurement (refer to paragraph 4.34).

2. Substitute known capacitance values until a maximum return loss is obtained. A return loss of 33 dB or greater indicates that the unknown capacitance is within ±5% of the reference capacitance. If the return loss exceeds 46 dB, then the unknown and reference capacitances are within ±1% of each other. Refer to Table 4–2.

NOTE

The trace moves downward (increasing return loss) as the reference capacitance approaches the unknown capacitance. A change from a downward motion to an upward motion indicates that the reference capacitance value has passed the unknown capacitance value (either from a higher value to a lower value or from a lower value to a higher value).

4.66 CABLE LENGTH MEASUREMENT

4.67 The Level Tracer can be used to determine non-loaded cable length by either measuring: (1) the open circuit capacitance, and/or (2) the short circuit resistance of the cable under test. The measured parameter (capacitance or resistance) is then divided by the capacitance- or resistance-per-unit-length appropriate for the cable under test to calculate the cable length. The same techniques can determine the distance to an open or to a short circuit fault along a cable.

4.68 Measuring Cable Length, Open Circuit Capacitance Method

4.69 Any one of the three capacitance measurement techniques (paragraph 4.60) may be used on non-loaded cables. It is recommended that the return loss method be used since it is the most accurate and has the widest measurement range.

1. Connect the cable under test to the RECEIVE section LINE 1 connectors and a precision variable capacitance (not required for capacitance measurement—method 1) to the RECEIVE section LINE 2 connectors.

2. Ensure that the far end of the cable is open—circuited.

3. Measure cable capacitance using the return loss method (paragraph 4.65), the comparison method (paragraph 4.64), or the conversion chart method (paragraph 4.63).

4. Divide the measured capacitance by the appropriate value of cable capacitance-per-unit-length. Use of the nominal per-unit-length values yields a good approximation of the cable length. However, manufacturing tolerances and effects of temperature influence the overall accuracy. Figure 4–8 may be used to convert capacitance into equivalent cable length of 0.083 uF/mile or 0.066 uF/mile cable.

4.70 Measuring Cable Length, Short-Circuit Resistance Method

4.71 Either of the two resistance measurement techniques (paragraph 4.56) may be used on non-loaded cables. It is recommended that the return loss method be used since it is the most accurate and has a wider measurement range.

1. Connect the cable under test to the RECEIVE section LINE 1 connectors.

2. Ensure that the far end of the cable is short-circuited.

3. If using the return loss method, connect a precision variable resistance to RECEIVE section LINE 2 connectors.

4. Measure cable resistance using the return loss method (paragraph 4.59), or the impedance method (paragraph 4.58).

5. Divide the measured resistance by the appropriate value of cable resistance-per-unit-length for the cable under test (refer to Table 4–3). The calculated result gives the approximate cable length. Manufacturing tolerances and temperature effects influence the overall accuracy of the cable length determination.

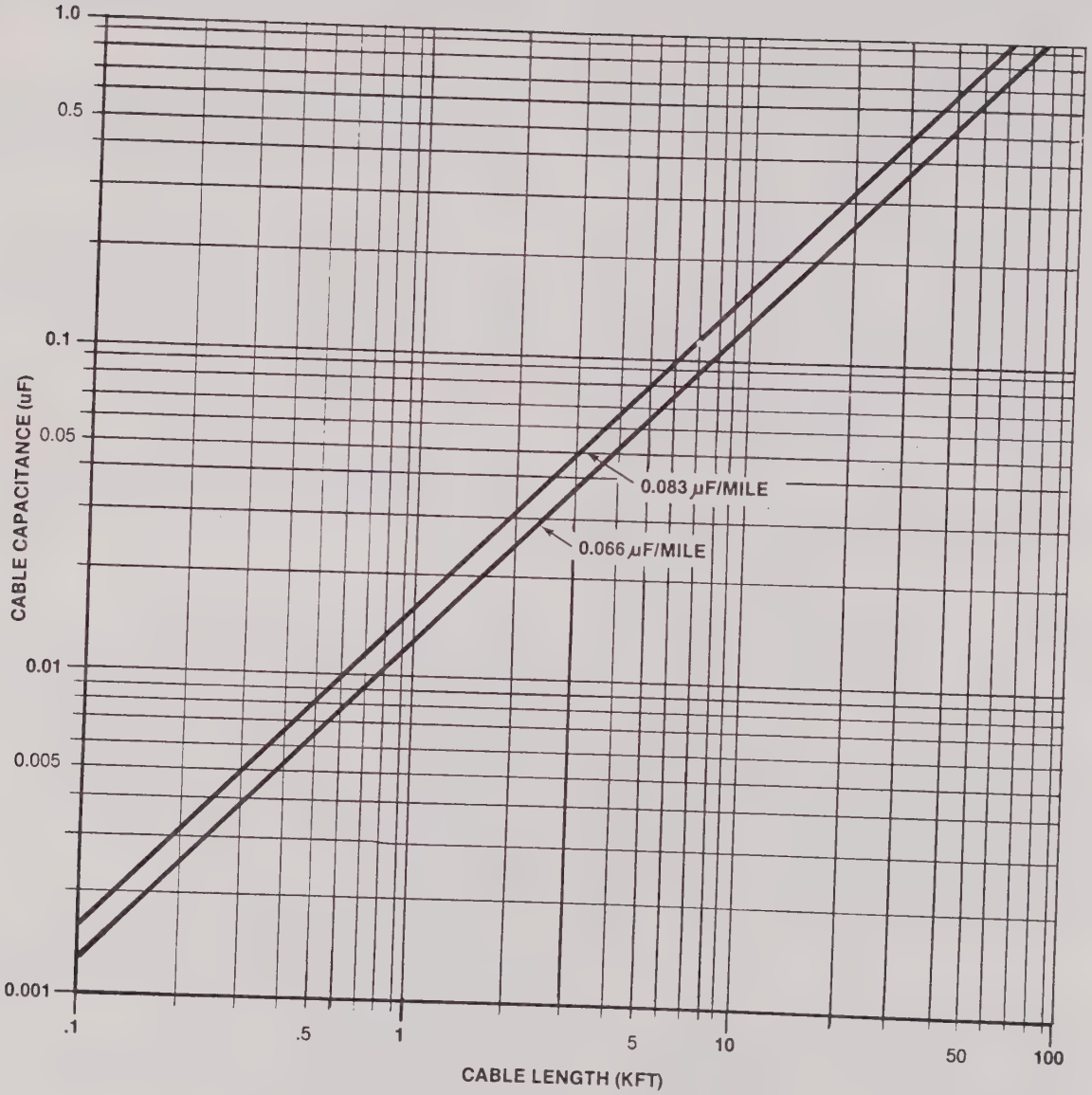


Figure 4—8. Capacitance To Cable Length Conversion

Table 4—3. Cable And Wire Resistance

FACILITY	GAUGE (AWG)	OHMS/KFT
CABLE		
Polyethetene	26	83.3
insulated	24	51.9
	22	36.6
	19	16.3
Paper	16	8.71
insulated	13	4.36
Distribution		
Urban	24	60.0
Suburban	22	34.8
Rural	19	17.4
UG Service, Rubber	19	17.4
WIRE		
C Rural Wire		
Steel	.083"	23.3
CWS	14	15.5
CWS	12	10.8
Drop Wire		
CWS	18	24.2
CWS	17	16.0
Bronze	17	16.0

4.72 FREQUENCY SHIFT MEASUREMENT

4.73 When a tone experiences a change in frequency during transmission over a circuit (often via carrier facilities), the circuit is said to have a frequency shift. The Level Tracer's frequency counting capability can be used to measure this parameter.

4.74 One Level Tracer can be used to transmit a known frequency into a circuit while another Level Tracer measures the received frequency at the other end of the circuit. Or, if the frequency of a milliwatt test line is accurately known and stable, frequency shift can be measured by a single Level Tracer after the circuit under test has been dialed to the test line.

4.75 CIRCUIT BALANCE MEASUREMENT

4.76 The balance of a circuit is a major factor in determining the circuit's communications performance, particularly susceptibility to induced noise. The balance of a circuit can be found by a calculation using noise measurement values obtained with the Level Tracer. Typical acceptable limits for noise levels are shown in Table 4—4.

4.77 Perform the following steps.

1. Store, display, and hold in a trace memory the metallic noise of the circuit under test (refer to paragraph 4.32).

2. Store, display, and hold in the other trace memory the noise to ground of the circuit under test (refer to paragraph 4.33).

3. The circuit balance is as follows:

BALANCE = (noise to ground) − (metallic noise)

For example:

Noise to ground = 78 dBrnC
Metallic noise = 13 dBrnC
Balance = (78) − (13) = 65 dB

Table 4—4. Typical Noise Limits For Cables

QUALITY	NOISE (METALLIC) dBrnC	NOISE TO GROUND dBrnC	BALANCE dB
GOOD	20	80	60
MARGINAL	20-30	80-90	50-60
BAD	30	90	50

4.78 THROUGH AND TERMINAL BALANCE APPLICATIONS

4.79 Through balance and terminal balance refer to the process of measurement, adjustment, and evaluation used to control echo and singing in the switched network. The balancing procedures in this manual are presented in general terms, without regard to specific types of switching equipment, testing arrangements, or office layout. This has been done to highlight the use of the Level Tracer in balancing procedures. Reference should be made to applicable practices for specific procedures. Knowledge of echo and singing phenomena, the switched network hierarchy and via-net-loss design are assumed.

4.80 Before balance tests and adjustments are made, some preliminary work is necessary. Apparatus installation must be verified . . . the various types of cross-office paths should be sketched, and records prepared. The 1004-Hz loss of trunk relay equipment to be balanced must be measured. Balance measurements are of no value unless the 1004-Hz loss requirements are met.

4.81 Preparatory work for terminal balance includes verification that outside plant cable acceptance testing is complete . . . impedance compensation done . . . 2-dB pads are installed where required . . . impedance matching provided where needed. Preliminary work for terminal balance also includes checking repeating coils for proper turns ratios . . . midcoil capacitance . . . and correct orientation of ratios.

4.82 **Through Balance**

4.83 Intertoll trunking is normally via 4-wire facilities. At 2-wire control switching points, 4-wire terminating sets (4-WTS) convert the 4-wire trunks to 2-wire for switching purposes. After switching is completed, the 2-wire trunks are reconverted to 4-wire facilities.

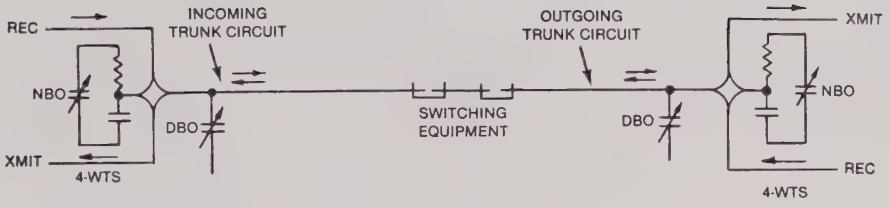
4.84 The amount of echo returned at these conversion points depends on the impedance present at the 2-wire side of the terminating set. The impedance in turn depends on the amount of office cable from the incoming terminating set through the switching equipment to the outgoing terminating set. The procedure used to control the impedance is called through (or office) balance.

4.85 The primary purpose of through balance is to make the impedance of all possible paths through the switching equipment nearly the same in order to prevent objectionable echo. Figure 4—9 shows several typical paths through a 2-wire control switching point.

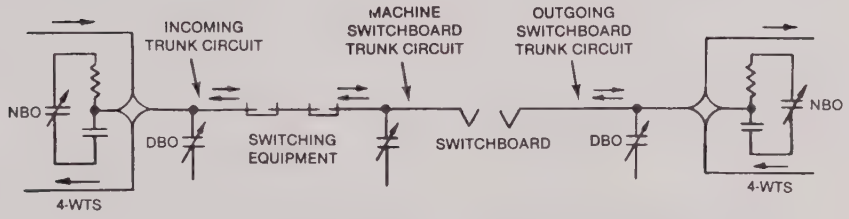
4.86 Through balance is measured from one 4-wire terminating set through the office switching equipment and wiring to the other 4-wire terminating set of each possible connection. Through balance involves only the office equipment and does **not** include outside 4-wire facilities. The 4-wire facilities are disconnected at the 4-wire terminating set and replaced by resistance terminations during balance measurements.

4.87 To adjust an office for through balance, the first step is to establish the value which will be used for the network building out capacitor (NBOC). The longest cross-office path . . . the path with the greatest capacitance . . . determines the NBO capacitance. Such a path may involve an incoming trunk, a machine-to-switchboard trunk, and switchboard-to-machine trunk to an outgoing trunk. The longest of each of these trunk types is determined by visual inspection, office records, or bridge-type capacitance measurements. (Refer to paragraph 4.60.)

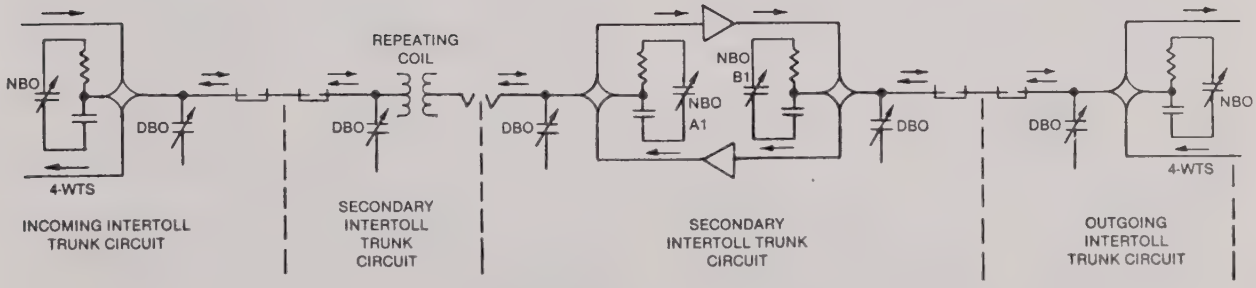
4.88 Next, cross-office capacitance measurements are made. A through connection is established for each possible configuration and a capacitance measurement is made as shown in Figure 4—10. The longest outgoing trunk is terminated at the 4-wire side and the Level Tracer is connected to the 4-WTS of the longest incoming trunk. The test setup is actually a 4-wire return loss setup.



A. INTERTOLL SWITCHING ROUTE THROUGH SWITCH MACHINE



B. INTERTOLL SWITCHING ROUTE THROUGH SWITCHBOARD



C. INTERTOLL SWITCHING ROUTE USING SECONDARY 4-WIRE TRUNK

Figure 4—9. Typical Intertoll Trunk Switching Paths

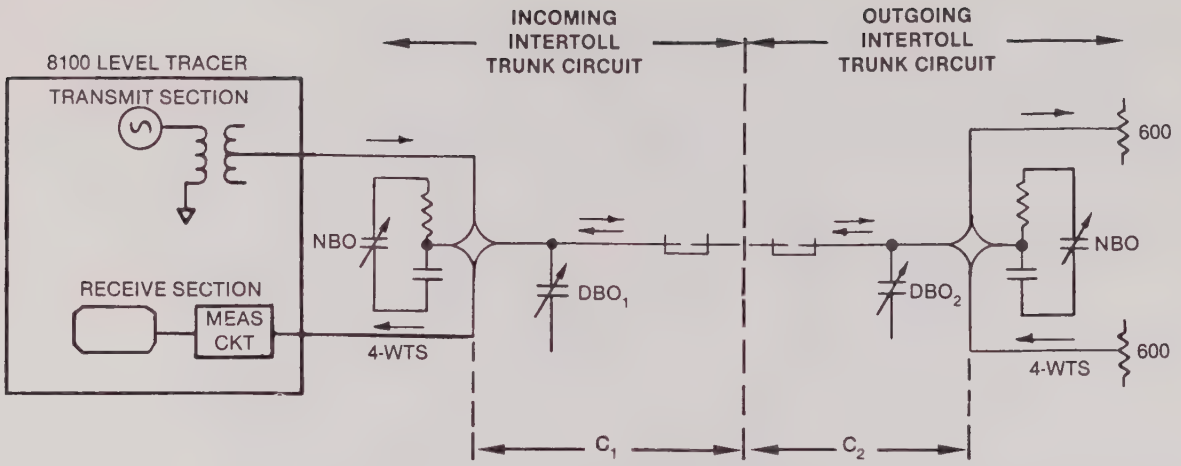


Figure 4—10. Measurement Of NBO Capacitance

4.89 The NBOC of the longest incoming trunk is typically adjusted for maximum return loss at 2000 Hz. The value of the largest NBOC represents the capacitance of the 2-wire line with the longest cross-office path of a through connection. This value, plus some allowance (usually 10%) for expansion, is chosen as the NBOC for the office.

NOTE

Measurements at 2000 Hz and higher are more accurate than those at a lower frequency because of the various series capacitors and bridged inductors which may be present in the trunk equipment. The impedance effects of these components are negligible at high voice frequencies. The office cabling capacitance is a shunt capacitance that is more easily measured at higher frequencies.

4.90 The chosen value of NBOC for the office is strapped into the balancing networks of all 4-WTS in the office. Then, drop building out capacitors (DBOC) must be adjusted on all trunks in the office under the same test configurations. The DBOC of each incoming trunk is adjusted for maximum return loss, typically at 2000 Hz, when the trunk under test is connected either to the longest incoming trunk or to a test termination. The test termination must first be built out to simulate the longest outgoing trunk (see Figure 4—11). Figure 4—12 illustrates the DBOC adjustments on an incoming trunk.

4.91 A reference incoming trunk is then connected (by dialing) to each outgoing trunk. The DBO capacitors of the outgoing trunks are adjusted for maximum return loss as shown in Figure 4—13.

4.92 Terminal balance is performed if also required by the office before completing through balance. To complete the balance work, after the NBO and DBO capacitors have been adjusted, several tests should be made on all trunks. Echo return loss (ERL) and singing points (SP) must be measured to determine if the office meets through balance objectives.

4.93 The measurements of ERL and SP for an office are made on connections set up between the reference incoming trunk 4-WTS and the 4-WTS of every outgoing trunk. The test set up for ERL is similar to the set up shown in Figure 4—13 except that the Level Tracer supplies a weighted noise signal (Level Tracer SIGNAL switch set at ERL). A singing point test set is used to measure SP.

4.94 ERL measurements must include a correction factor to account for the transmission loss within the 4-WTS This is easily accomplished with the Level Tracer as follows.

1. Set up a 4-wire return loss test with the 2-wire port of the 4-WTS terminated by a short circuit.

2. Adjust the transmit level of the ERL signal as to obtain 0 dB on the Level Tracer display screen with the FUNCTION range select switch set at 0. Then LEVEL dBm switch settings equals the transmission loss of the 4-WTS.

3. Remove the short circuit and connect the trunk under test. Measure the level without changing the positions of the LEVEL dBm switches.

4. Position the trace on the Level Tracer as close as possible to the 0-dB reference line.

5. The algebraic sum of the FUNCTION range select switch position and the displayed level represents the echo return loss for the trunk under test.

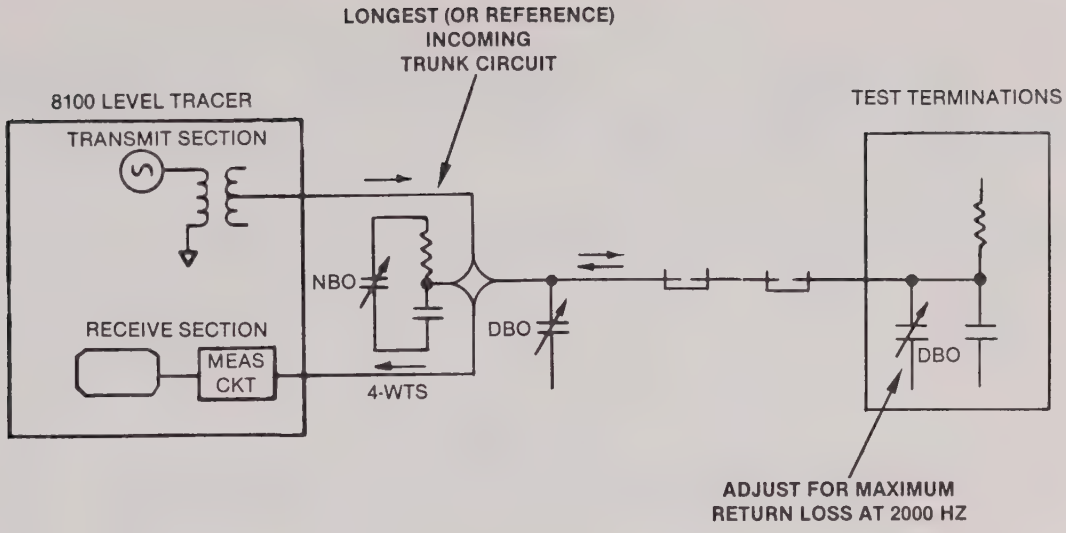


Figure 4—11. Adjustment Of DBO Capacitance On Test Termination

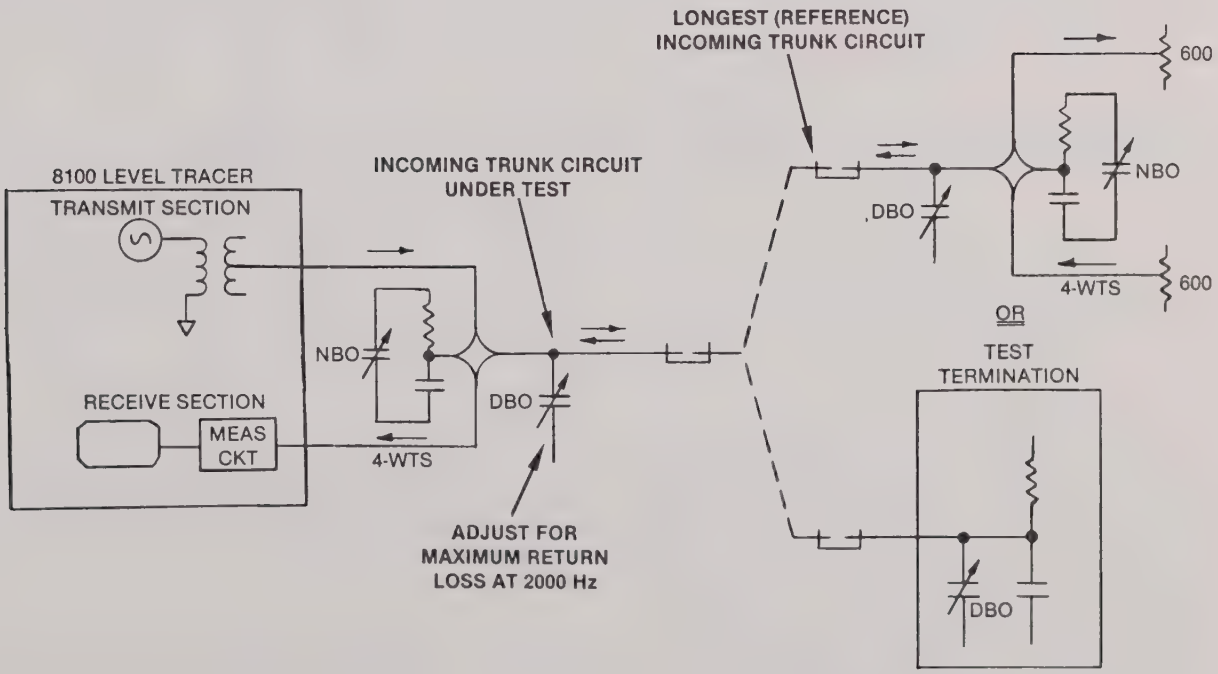


Figure 4—12. Adjustment Of DBO Capacitance On Incoming Trunk

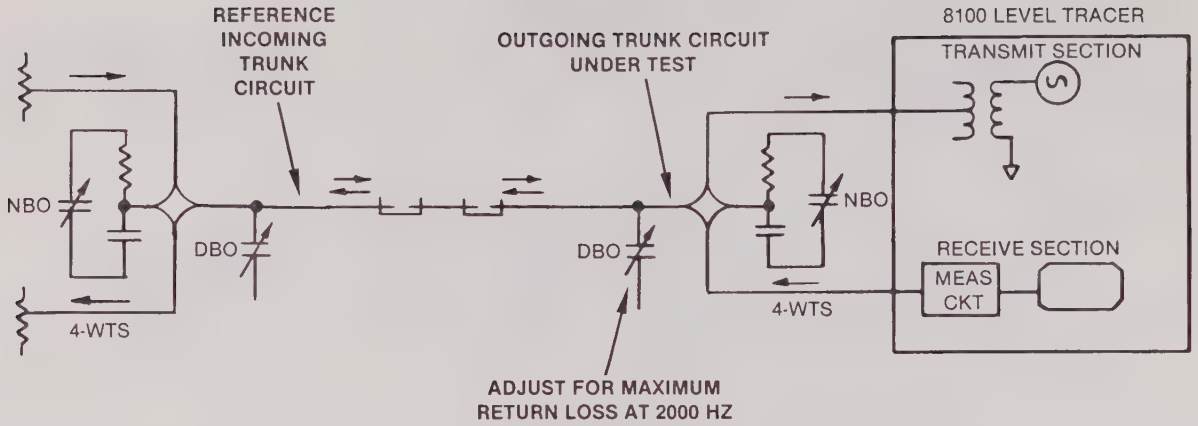


Figure 4—13. Adjustment Of DBO Capacitance On Outgoing Trunk

4.95 If the 4-WTS transmission loss exceeds 10 dB then the following alternate method may be used.

1. Set up a 4-wire return loss test with the 2-wire port of the 4-WTS terminated by a short circuit.

2. Set the level of the ERL signal to 0 dBm (LEVEL dBm switch settings of 0 and 0).

3. Record the received level.

4. Remove the short circuit and measure the level received with the trunk under test connected to the 4-WTS. Leave the transmit signal at 0 dB.

5. Record the received level.

6. The difference between the levels of steps 5 and 3 is the echo return loss of the trunk under test.

4.96 **Terminal Balance**

4.97 Terminal balance is defined as the balance between the impedance of the compromise network in the 4-WTS of the intertoll trunk and the impedance of the toll connecting trunk. The purpose of the terminal balance process, adjusting NBO and DBO capacitors, is to minimize the range (spread) of cross-office capacitance just as in through balance. But, the echo and singing return loss requirements are specified in the switched condition with the toll connecting trunk connected to a test termination in the class 5 office. Thus terminal balance **includes** the 2-wire facilities outside the class 4 office.

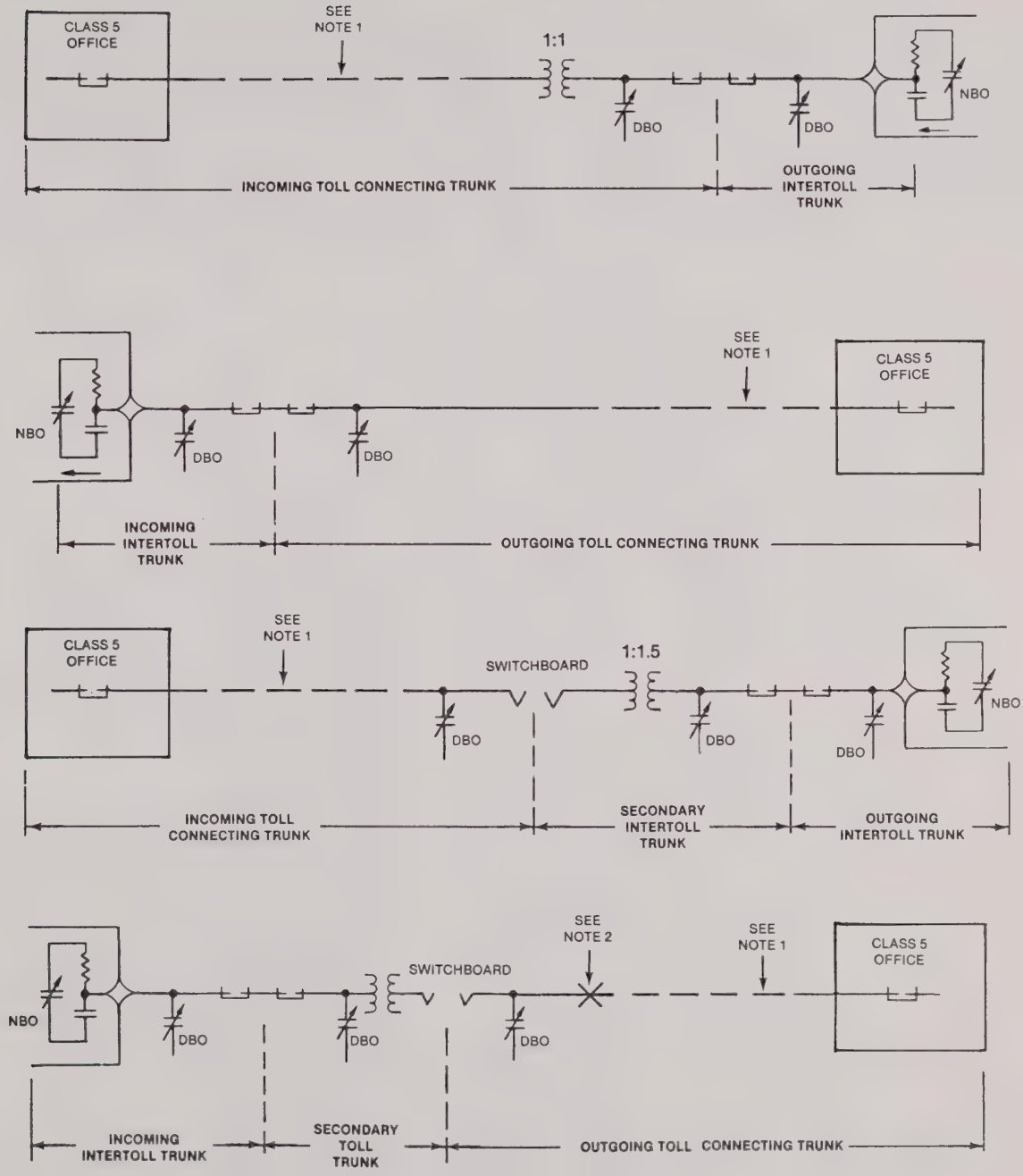
4.98 Figure 4—14 illustrates typical office connections that must meet terminal balance objectives. The first two examples show machine-switched connections and the last two examples include an operator switchboard connections.

4.99 In an office requiring terminal balance only, the average intertoll trunk-to-toll connecting trunk capacitance is determined and used as a compromise value for the office NBOC.

4.100 To obtain the compromise NBOC value, capacitance measurements are made on samples of the shortest and longest trunks of each type of toll connecting facilities. As shown in Figure 4—15, these may include 4-wire trunks, 2-wire loaded trunks with impedance compensation, or short non-loaded trunks with 2-dB pads. Each type of trunk may be subdivided further by type of signaling system and types of equipment and facilities used on the trunks.

4.101 If the range between the largest capacitance and the smallest capacitance is 0.025 uF or less, then the average between these two extreme values is used as the compromise NBOC value. Typically, no DBO capacitors are used when the measured capacitance range is 0.025 uF or less.

4.102 When the capacitance range is greater than 0.025 uF, the shorter paths are excluded from the determination of the compromise NBOC value. DBO capacitors are then added to the excluded paths to build them out to the compromise value.



NOTES:

1. INTEROFFICE FACILITIES:
   NON LOADED CABLE
   VF LOADED CABLE
   4-WIRE CARRIER
   2-WIRE REPEATED CIRCUIT
2. POINT OF TERMINATION FOR OFFICE CABLE BUILD OUT

Figure 4—14. Typical Terminal Balance Connections

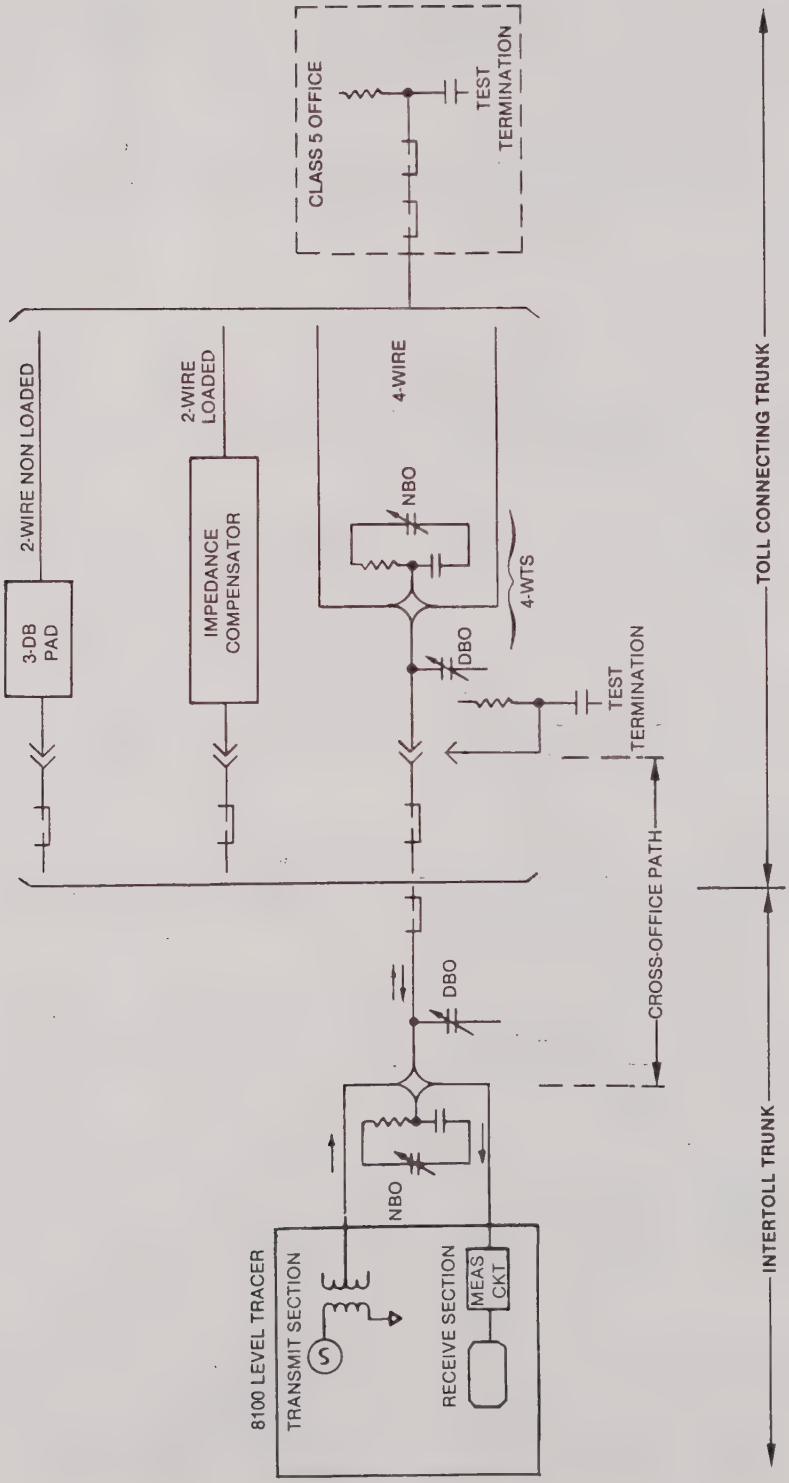


Figure 4—15. Terminal Balance Capacitance Measurement

4.103 Figure 4—16 illustrates the method used to determine the office NBOC and the trunk DBOC when the range of cross-office paths exceeds 0.025 uF. In the example shown, the longest path measured is 0.045 uF and the shortest path uF. All paths below 0.020 uF (0.010—0.020) are excluded. The midrange path then becomes (0.045 + 0.020)/2 = 0.0325. A capacitance value of 0.0325 is calculated but a capacitance value of 0.033 uF is chosen as the compromise NBOC for the office.

4.104 The DBOC value is determined by calculating the average capacitance of the excluded paths and subtracting the result from the compromise NBOC value. For the example shown in Figure 4—16, the compromise DBOC value is: 0.033 − (0.020 + 0.010)/2 = 0.018 uF. This value of DBO capacitance is added to each path below 0.020 uF to build it out approximately to the compromise value of 0.033 uF. Thus after terminal balance, the range in cross-office capacitance does not exceed 0.025 uF.

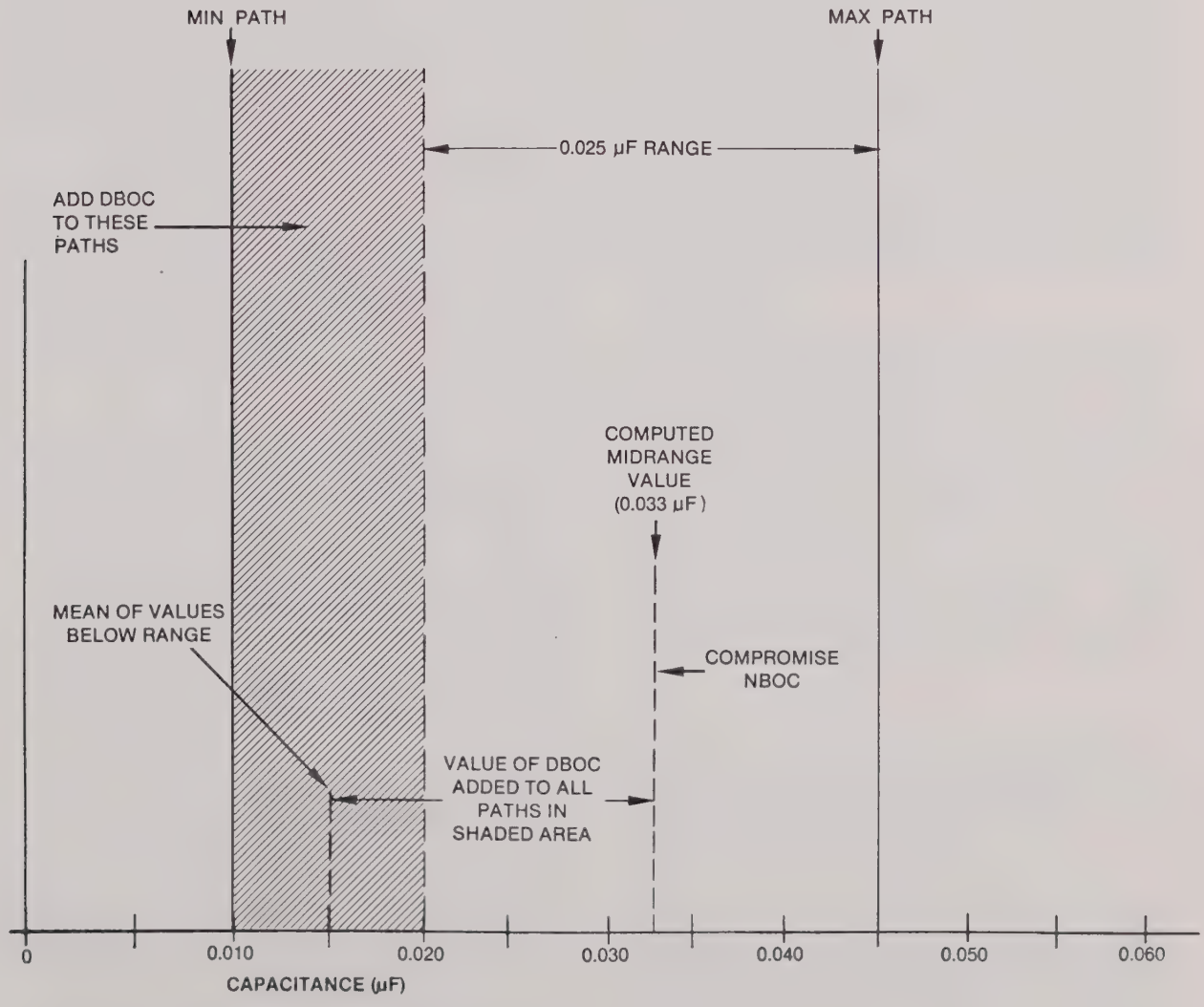


Figure 4—16. Determining NBO And DBO Capacitances For Terminal Balance (Class 4 Offices)

4.105 Capacitance measurements for terminal balance are made to test termination (600 or 900 ohms in series with 2.16 uF) with the toll connecting trunk disconnected at the point of termination. A connection is established to each toll connecting trunk to be measured from an average length incoming intertoll trunk. The NBOC on the intertoll trunk 4-WTS is adjusted for maximum return loss, typically at 2000 Hz, and the capacitance value is recorded. The compromise value of office NBOC is chosen from these measurements as previously described.

4.106 In offices requiring through balance as well as terminal balance, the NBOC value established for through balance is also used for terminal balance. It may be necessary to add DBO capacitance to some or all toll connecting trunks.

4.107 Samples of toll connecting trunks are selected for DBOC measurements. The DBO capacitors on the sampled trunks are adjusted for maximum return loss when the toll connecting trunks are connected to an intertoll trunk adjusted to meet through balance objectives. The DBOC value chosen for trunks of one specific type should be the arithmetic mean of the sample (the sum of the sampled capacitance divided by the sample size).

4.108 To complete terminal balance, ERL and SP measurements should be made on all toll connecting trunks. These measurements verify that the office meets terminal balance objectives. It is important to note that the paths measured for ERL and SP:

1. begin at the 4-WTS,

2. extend through the switching equipment of the toll office (class 4 or higher),

3. through (and including) the toll connecting trunk,

4. the class 5 switching machine, and

5. terminate in a balance test termination (900 ohms in series with 2.16 uF) in the class 5 office which homes on the toll office being measured.

4.109 STRUCTURAL RETURN LOSS

4.110 Poor structural return loss of a cable pair can degrade the terminal balance. The structural return loss is a measure of the impedance match between an ideal line (a precision network) and a working cable pair when the cable pair is terminated in a precision network. Structural return loss measurements must include all cable apparatus such as impedance compensators, pads, repeaters and of course all load coils. Manufacturing tolerances, wire gauges, load spacing . . . etc, all adversely affect the structural return loss.

4.111 Structural return loss measurements using the Level Tracer may be made using a weighted noise signal (ERL noise signal) or a sweep signal. The return loss of a cable pair made with an ERL noise signal is called the echo structural return loss (ESRL). When using a sweep signal, the frequency between 300 and 3000 Hz at which the poorest return loss occurs is known as the critical frequency structural return loss (CFSRL).

4.112 IMPEDANCE COMPENSATOR ADJUSTMENT

4.113 An impedance compensator makes the impedance of a loaded cable pair more uniform over the voice-frequency range and more nearly equal to the impedance needed at a toll-switching office. A basic impedance compensator consists of a fixed series inductance and a variable shunt capacitance. Impedance compensator may also contain low-frequency correctors and build-out resistors.

4.114 Nearly all loaded cable pairs are designed such that the distance to the first load point equals the length of one half of a full loading section. The impedance seen at the mid-point of a loading section varies as a function of frequency. The negative reactive component is essentially constant, but the resistive component is frequency sensitive.

4.115 The capacitance of the impedance compensator is used to lengthen (build-out) the office end section of a loaded cable to 0.8 of a full loading section. This changes the previous impedance to an impedance whose resistive component is now essentially constant with frequency but whose reactive component changes with frequency. The positive reactance of the series inductance compensates for the negative reactance due to the added capacitance. Thus the reactive component varies over a narrower range than before, and the impedance is nearly insensitive to frequency change over the voice band.

4.116 Figure 4—17 shows a test set up for determining the build out capacitance used in impedance compensators. Trunks with similar characteristics (trunks in the same loading complements) are tested on a sampling basis. Then the measured build out capacitance values are averaged. The BOC capacitors of the impedance compensators for all trunks covered by the sample are set to this one average value.

4.117 If a voice-frequency repeater is used in an intermediate office, verify that the repeater is actually in the trunk and functioning at its specified gain. Then perform the following steps.

1. Make a selection of several trunks (a random sample) using impedance compensators and working in the same trunk cable loading complement. Remove the trunk to be tested from service.

2. Select the proper precision balancing network settings for use in the class 5 office.

3. At the class 5 office main distributing frame (MDF) open the trunk under test. To the outside cable conductors at the MDF, connect the precision balancing network (PBN) and decade capacitor box. Disconnect any built-in BOC capacitor if present in the precision balancing network so that all of the build out capacitance is obtained directly from the decade capacitor box.

4. Set the decade capacitor box to a preliminary value equal to the average full load section capacitance minus the actual (class 5 office) end-section capacitance and minus the network basic end-section capacitance.

5. At the toll-switching office, disconnect the cable wires and the low-frequency corrector (if any) from the office side of the impedance compensator. Connect a capacitor decade box across the tip and ring terminals on the cable side of the impedance compensator. Disconnect the BOC inside the impedance compensator so that all of the build out capacitance is obtained directly from the decade capacitor box.

6. Connect the office side of the impedance compensator to the Level Tracer LINE 1 TIP and RING connectors. Connect a compromise network (900 ohms in series with 2.16 uF) to the Level Tracer LINE 2 TIP and RING connectors.

7. When a voice-frequency repeater is equipped with a repeater disabler, and is used on the trunk, block the enabler relay in operate position.

8. Set up the Level Tracer for a 2-wire return loss measurement (refer to paragraph 4.43) with a sweep signal. (A fixed tuned 2500 Hz signal may also be used.)

9. Adjust the decade capacitor box at the toll-switching office for maximum return loss in the 2000 Hz to 3000 Hz range as shown on the Level Tracer display screen.

10. Adjust the decade capacitor box at the class 5 office for maximum return loss in the 2000 Hz to 3000 Hz range as shown on the Level Tracer display screen.

11. Repeat steps 9 and 10 until no further improvement in return loss is obtained by a change in either of the capacitor decade boxes.

12. Record the dial settings of the decade capacitor box at the toll-switching office.

13. Remove all test connections including the relay blocking tool (step 7). Reconnect all cable wires and return the trunk to service.

14. Repeat steps 1 through 13 on the other trunks selected for test.

15. Calculate the average capacitance value for all the trunks tested. The result is the build out capacitance value required in the BOC capacitor for each impedance compensator of all the trunks associated with the sample group.

16. Strap the calculated average capacitance value in all the impedance compensators working in this trunk loading complement. Working trunks should be taken out of service when strapping impedance compensators. Restore each trunk to service as soon as possible.

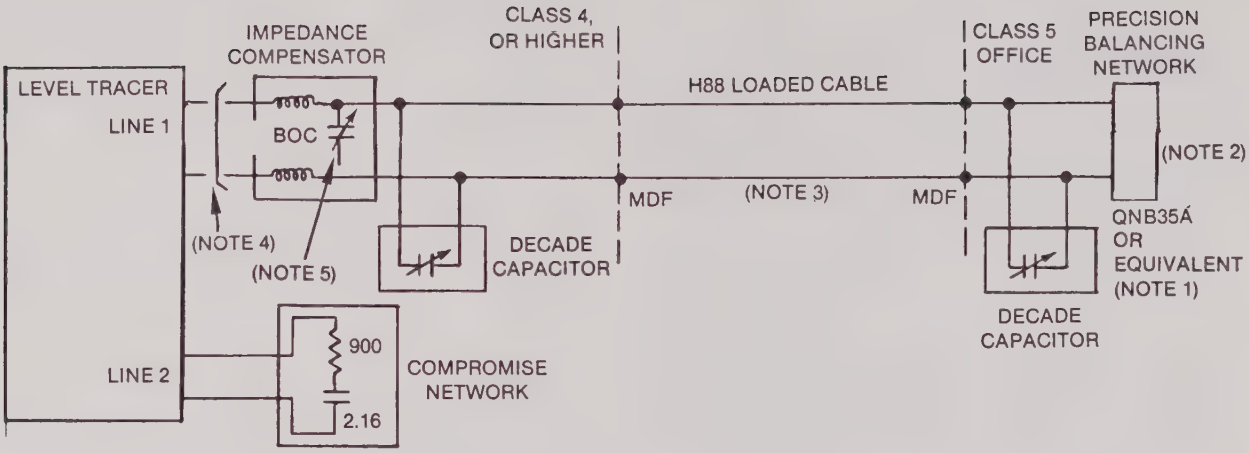
17. Select the next random sample from the next trunk cable loading complement. Repeat steps 1 through 16. Continue in a similar manner until all impedance compensators in each trunk cable loading complement have been adjusted.

4.118 FAULT LOCATION ON CABLE PAIRS USING IMPEDANCE MEASUREMENTS

4.119 When a cable pair is terminated in its characteristic impedance, the cable pair appears to be infinitely long, and the cable's characteriestic impedance will appear at the sending end. When the terminating impedance has some other value, the sending end impedance will be a function of both the cable pair impedance and the terminating impedance. If a cable pair has an irregularity, the pair's characteristic impedance is changed. This forms the basis by which faults may be diagnosed using the Level Tracer.

4.120 The Level Tracer used in conjunction with an artificial line can help locate faults in cable pairs. Comparison of the impedance curve of a cable pair with the impedance curve of a similar artificial line provides clues which help identify and locate faults.

4.121 Impedances are complex quantities having phase angles as well as magnitudes. The Level Tracer measures only the impedance magnitude and cannot measure the phase angle.Therefore, further discussion will be concerned only with the magnitude (absolute value) of impedance.



NOTES:

1. NORTHERN TELECOM, INC. PRECISION BALANCING NETWORK QNB35A IS EQUIVALENT TO TYPE 115 NETWORK
2. SET PRECISION BALANCING NETWORK SWITCHES PER MANUFACTURER'S RECOMMENDATION FOR GAUGE AND END SECTION LENGTH OF CABLE. DISCONNECT ANY INTERNAL BOC
3. WHERE A VOICE-FREQUENCY REPEATER IS USED IN AN INTERMEDIATE OFFICE, THE REPEATER MUST BE CONNECTED INTO THE TRUNK AND OPERATING AT SPECIFIED GAIN. WHERE REPEATER DISABLERS ARE USED, BLOCK THE ENABLER RELAY IN OPERATE POSITION.
4. DISCONNECT THE OFFICE CABLE WIRES AND THE LOW-FREQUENCY IMPEDANCE CORRECTOR (IF ANY) FROM THE OFFICE SIDE OF THE IMPEDANCE COMPENSATOR
5. DISCONNECT THE BOC SO THAT ALL OF THE BUILD OUT CAPACITANCE IS DIRECTLY OBTAINED FROM THE DECADE CAPACITOR

Figure 4—17. Adjustment Of Impedance Compensators

NOTES

All impedance curves shown were obtained using an artificial line to simulate a 22 gauge H88 loaded cable with five load coils. Unless otherwise specified, the full sections are 6 kft the end sections are 3 kft. In the cable schematics given with the impedance curves: a ( ) represents a load coil, a ( ) represents a double load coil, a ( ) represents one-half a load coil, a ( ) represents an open circuit, and a ( ) represents a short circuit.

4.122 Usually, an open circuit at the far end is a convenient condition for working purposes. A cable pair or circuit may be normally open or can easily be made open. For normally open condition, assistance is not needed at the far end. For normally terminated condition, it is often only necessary to have the termination removed by removing heat coils.

4.123 Open circuit impedance curves have typical shapes. Figure 4—18 shows the impedance curves for various lengths of non loaded cable. For comparison, the impedance curves for similar cable lengths with a short circuit at the far end are shown in Figure 4—19. Note that, for the open circuit condition, the point at which the trace crosses the uppermost line moves toward the right as the cable length decreases. For the short circuit condition, the trace moves downward as the cable length decreases.

4.124 Figure 4—20 shows open circuit impedance curves for an H88 loaded cable pair with five load coils and various far end section lengths. Observe that the peaks and dips are uniform and tend to rise smoothly toward the high frequencies. In addition, note that the last peak decreases in size and disappears as the far end section becomes shorter. For comparison, Figure 4—21 shows the short circuit impedance curves for the same cable pairs. Figure 4—21F clearly shows the difference between open and short circuit impedances. Observe the "phase" reversal that exists at low frequencies. At high frequencies, the two curves are back "in-phase" with each other.

4.125 Loading irregularities tend to upset the uniformity of the peaks and dips of open circuit impedance curves. This is illustrated in Figure 4—22 which shows the effects of a missing load coil at various loading points. Half load coils (see Figure 4—23) and doubled load coils (see Figure 4—24) also produce these types of impedance irregularities.

4.126 Note, in Figure 4—22F and 4—24F, that the impedance curves slope downward toward the high frequencies when the first load or a first half load coil is missing. This is a typical result whenever the CO end section has excessive capacitance. Long CO end section (see Figure 4—25) produce similar results, while bridged taps (see Figure 4—26) in the CO end section cause identical results. A build-out capacitor can also produce the same effects.

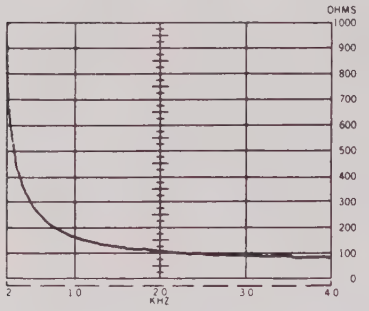
4.127 Just as the cause of excessive capacitance in the CO end section cannot be determined by open circuit impedance only, neither can the cause of excessive capacitance in the far end section. Figure 4—27 shows that the impedance curves of 3 kft bridged tap at various locations within the far end section are identical with each other and with Figure 4—20A. In addition, observe that the 1.5 kft bridged tap on a 3kft end section (Figure 4—27D) has a response curve identical to that of a cable pair with a 4.5 kft end section (Figure 4—20B).

4.128 Incorrect length of a full section also produces impedance irregularities just as improper end section lengths do. Figure 4—28 and 4—29 show the effects of length variations in a full section. Note that a bridged tap or a build-out capacitor would cause similar results shown in Figure 4—28A and 4—29A.

4.129 It is difficult to set hard rules for interpretation of all aspects of loaded cable pair impedance curves. The number of peaks and dips is determined by the number of loads, the far end section length, the cut off frequency, and the insertion loss. Generally speaking, the impedance curve should have peaks and dips that rise smoothly toward the high frequencies. When irregularities are observed, return loss and insertion loss tests may be necessary to determine and locate the fault.

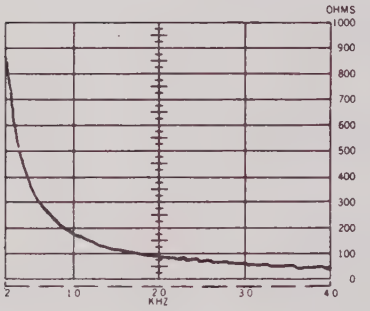
4.130 The pattern of curves for H88 loaded cable pairs does **not** apply to other loading plans, such as D66, since the Level Tracer frequency range is 4 kHz. The open circuit impedance is dependent on velocity of propagation and insertion loss.

22 GA NON-LOADED CABLE SCALE: X5



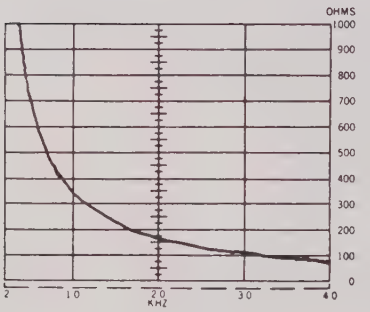
A

18KFT



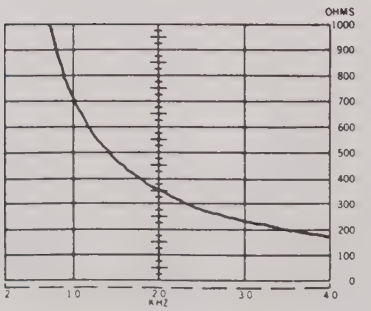
B

12 KFT



C

6 KFT

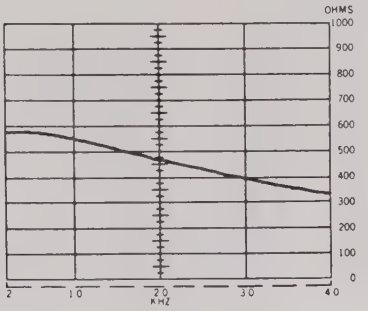


D

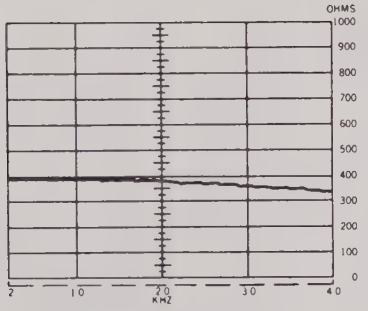
3 KFT

Figure 4—18. Open Circuit Impedance Of 22 GA Non-Loaded Cable

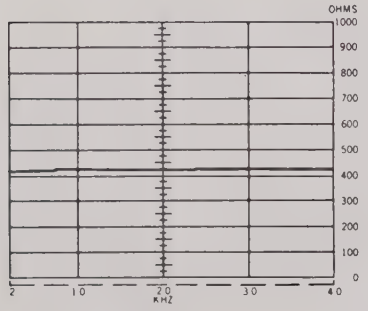
22 GA NON LOADED CABLE SCALE: X1



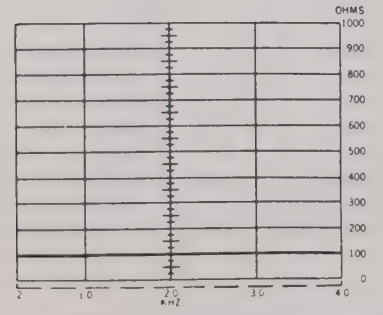
18 KFT



12 KFT



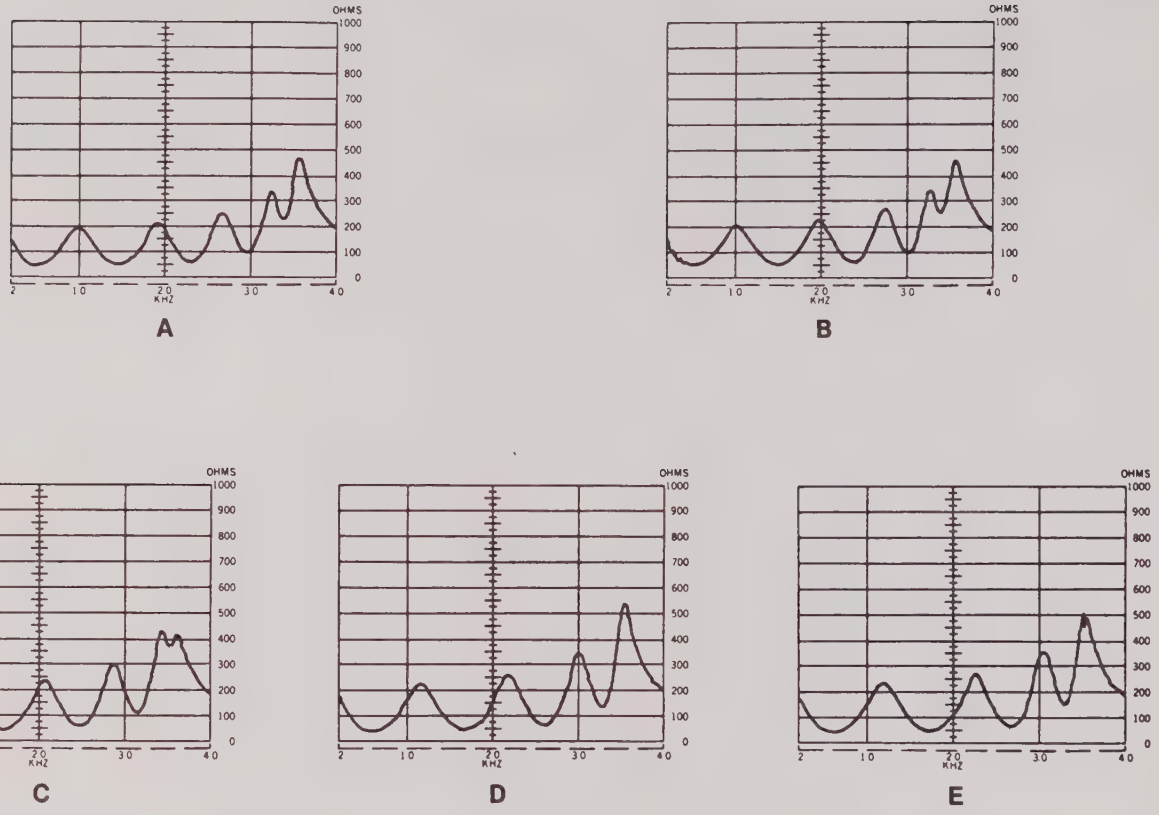
6 KFT



3 KFT

Figure 4—19. Short Circuit Impedance Of 22 GA Non-Loaded Cable

27 TO 33 KFT 22H88 LOADED CABLE SCALE X10



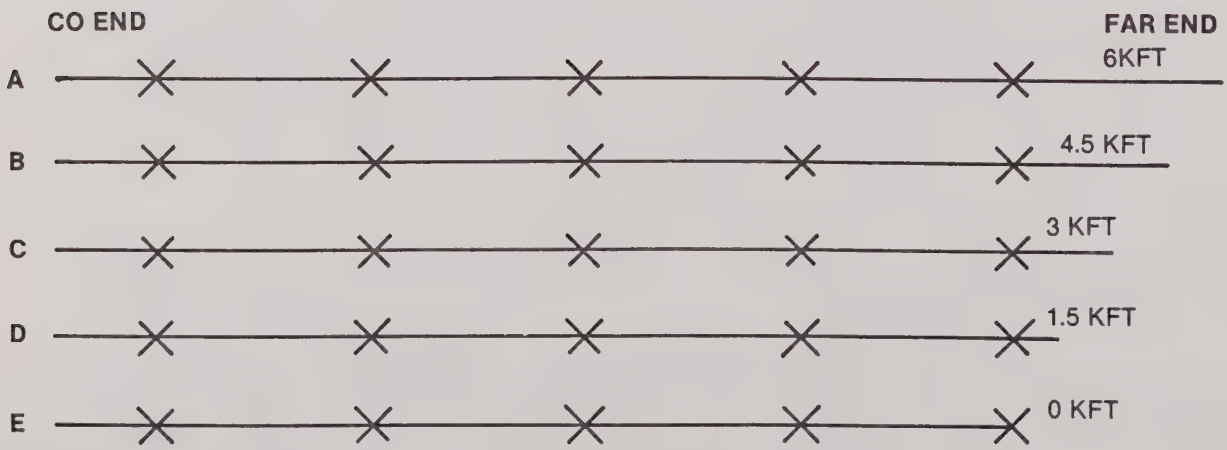
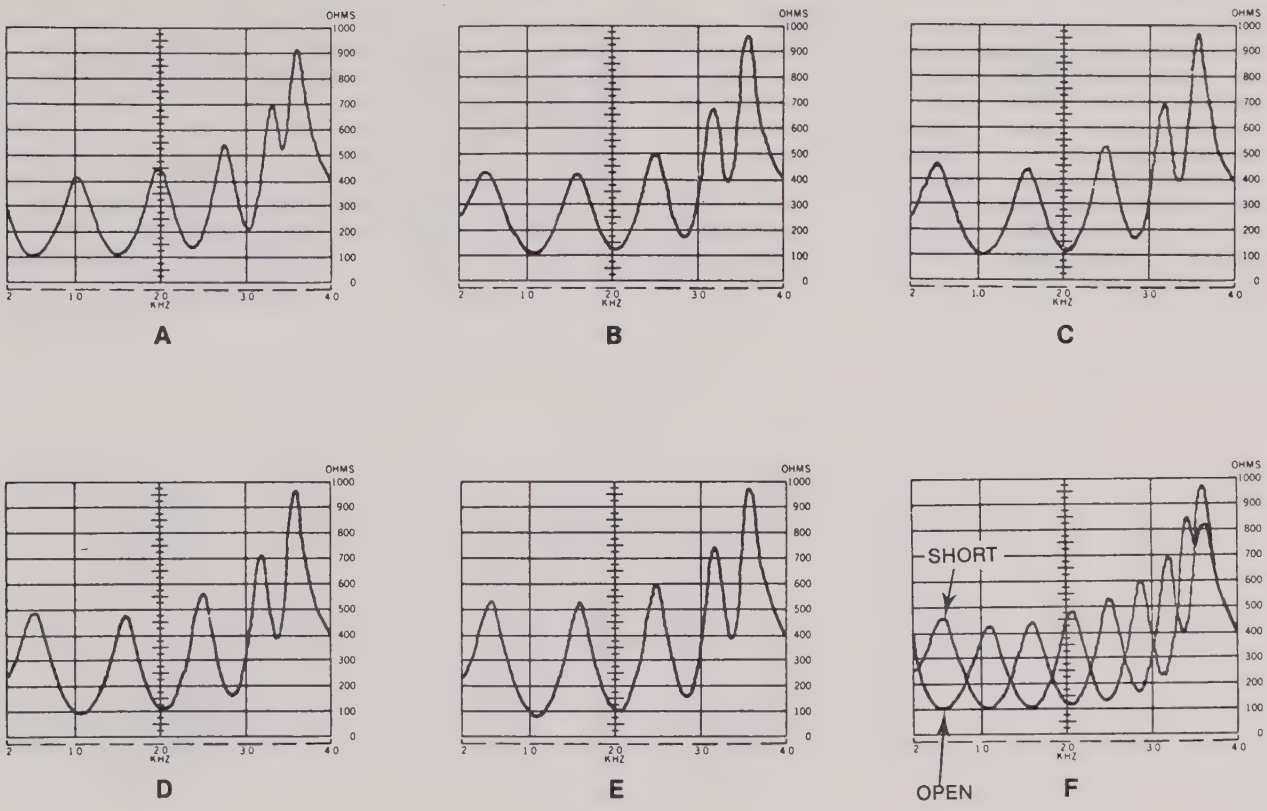


Figure 4—20. Effects Of Length Variations In Far End Section

27 TO 31.5 KFT 22H88 LOADED CABLE SCALE: X5



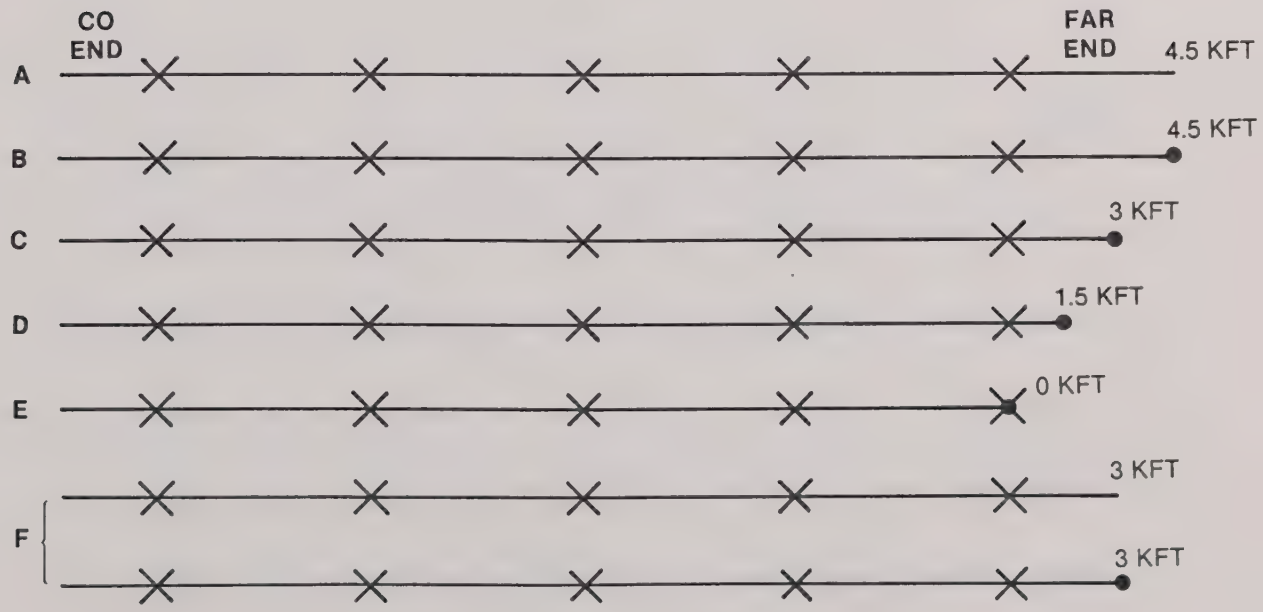
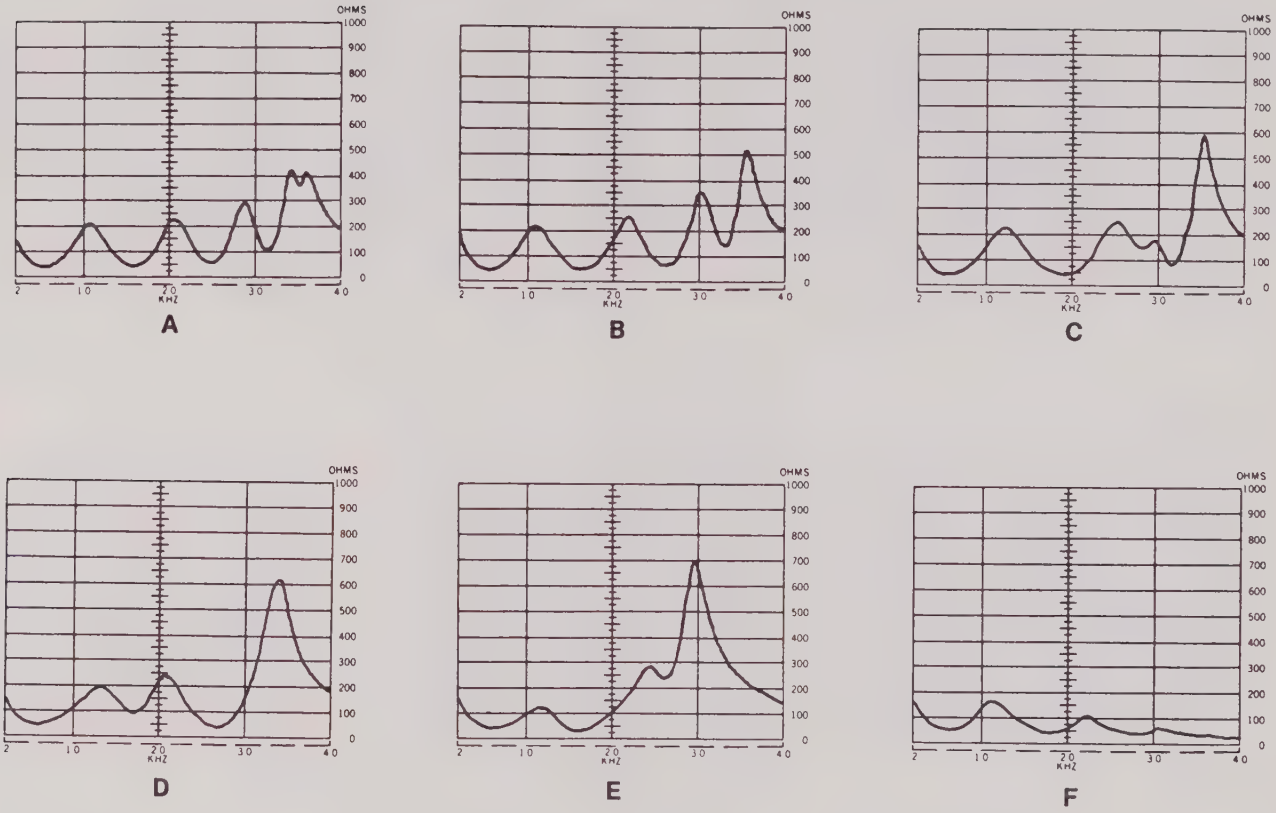


Figure 4—21. Effects Of A Short At Various Positions In The Far End Section

30 KFT 22H88 LOADED CABLE SCALE X10



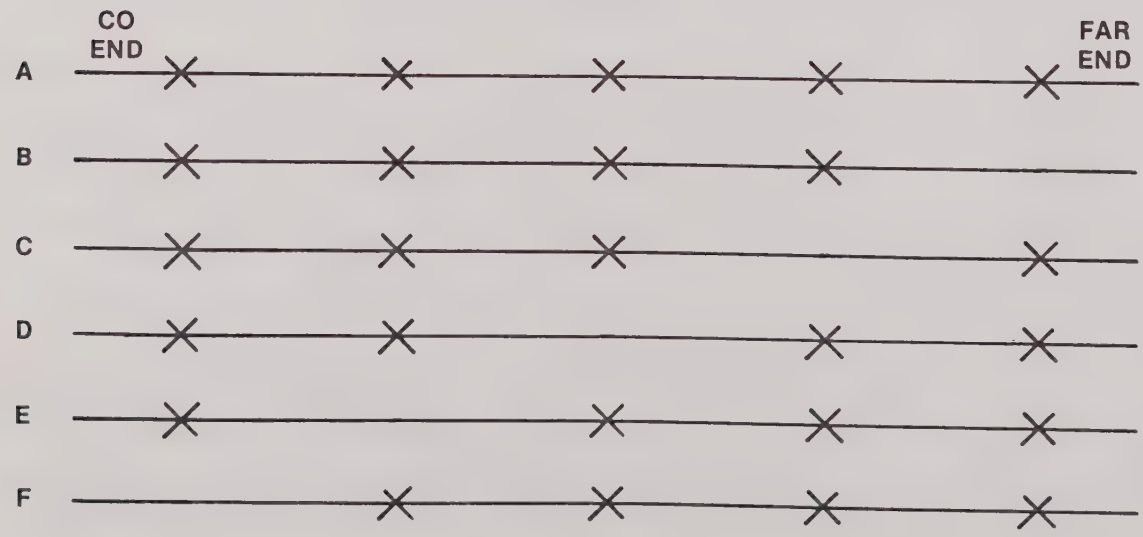
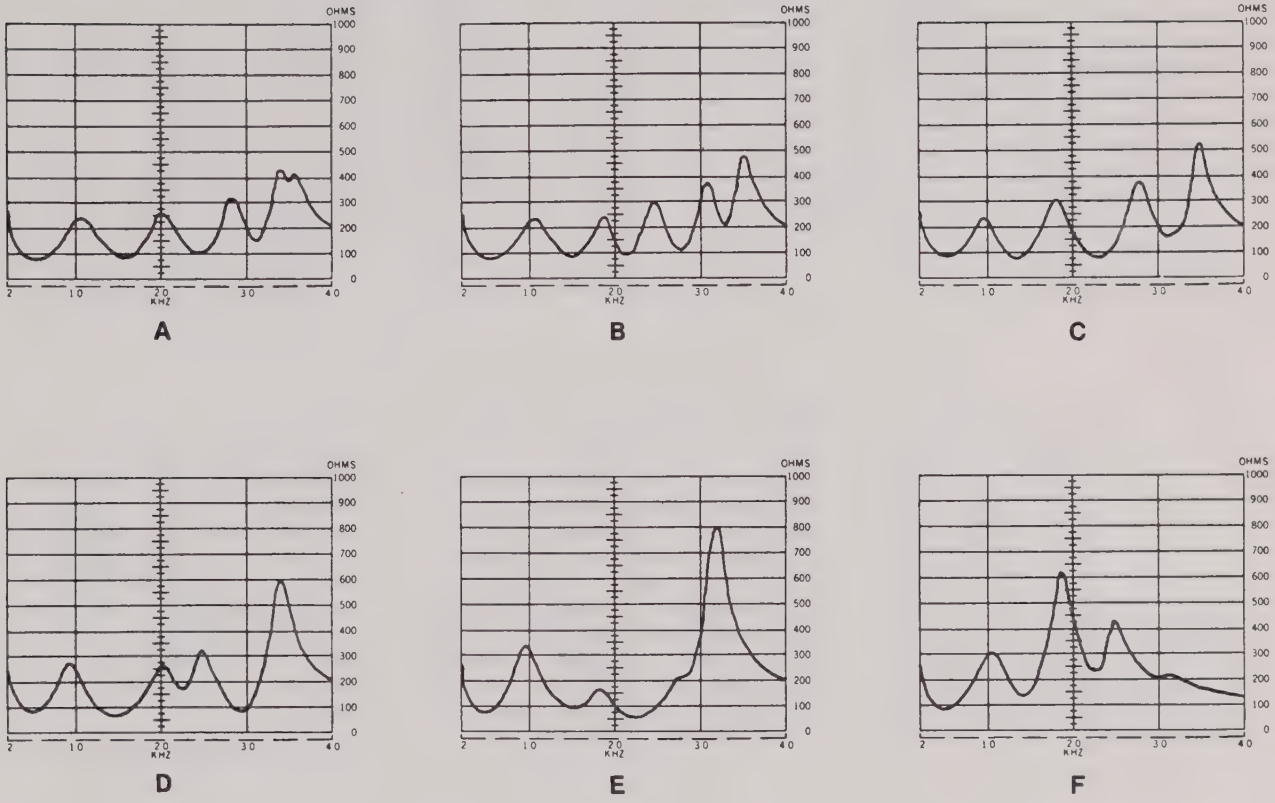


Figure 4—22. Effects Of A Missing Load Coil At Various Locations

30 KFT 22H88 LOADED CABLE SCALE: X10



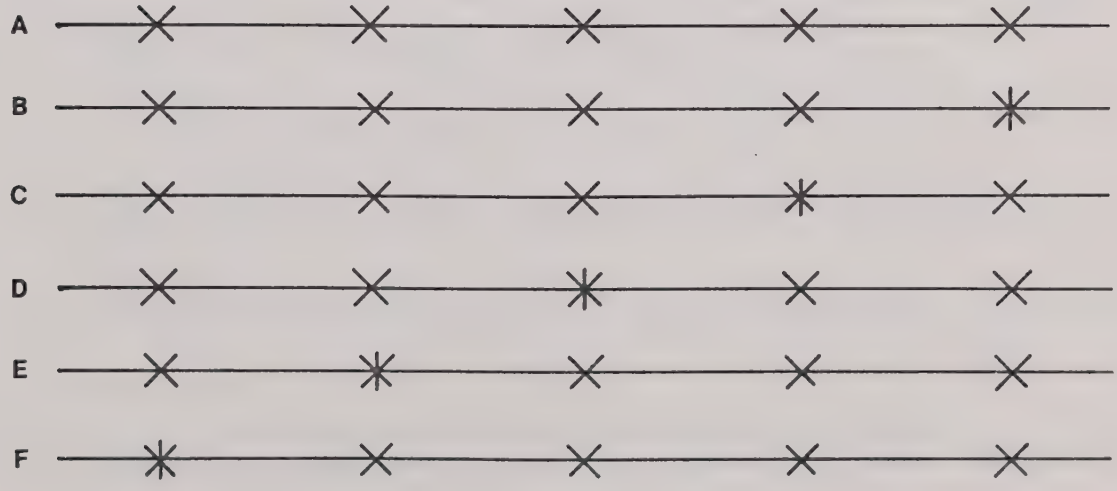
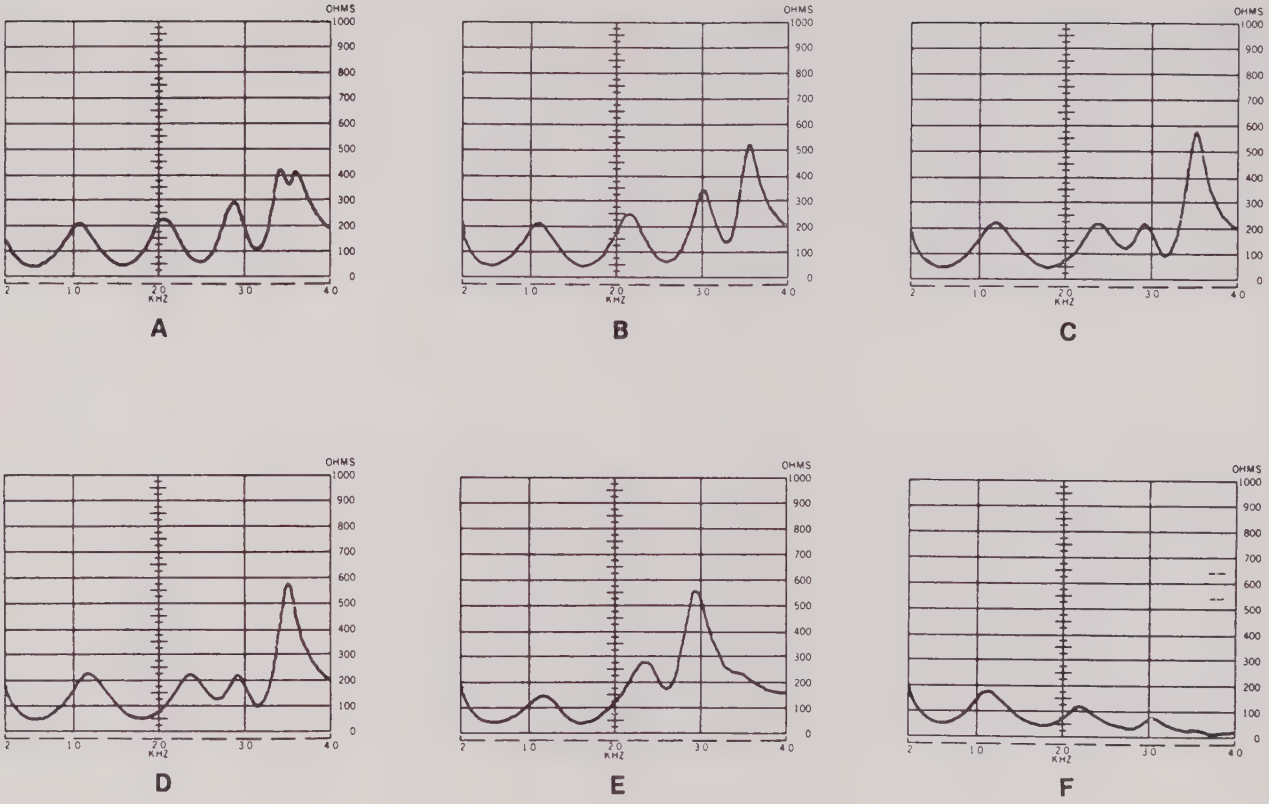


Figure 4—23. Effects Of A Doubled Load Coil At Various Positions

30 KFT 22H88 LOADED CABLE SCALE X10



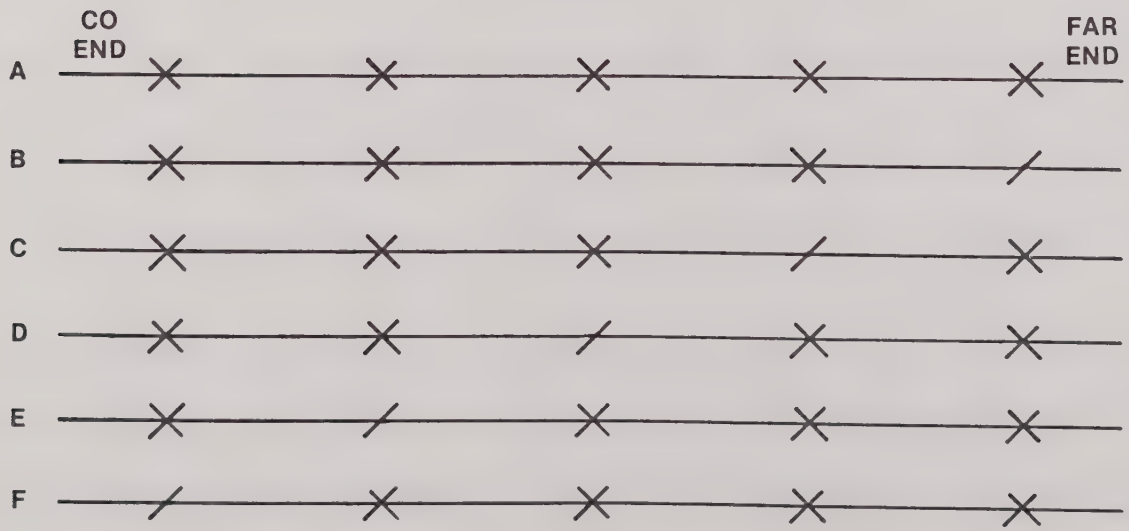


Figure 4—24. Effects Of One-Half Load Coil Missing At Various Positions

27 TO 33 KFT 22H88 LOADED CABLE SCALE: X10

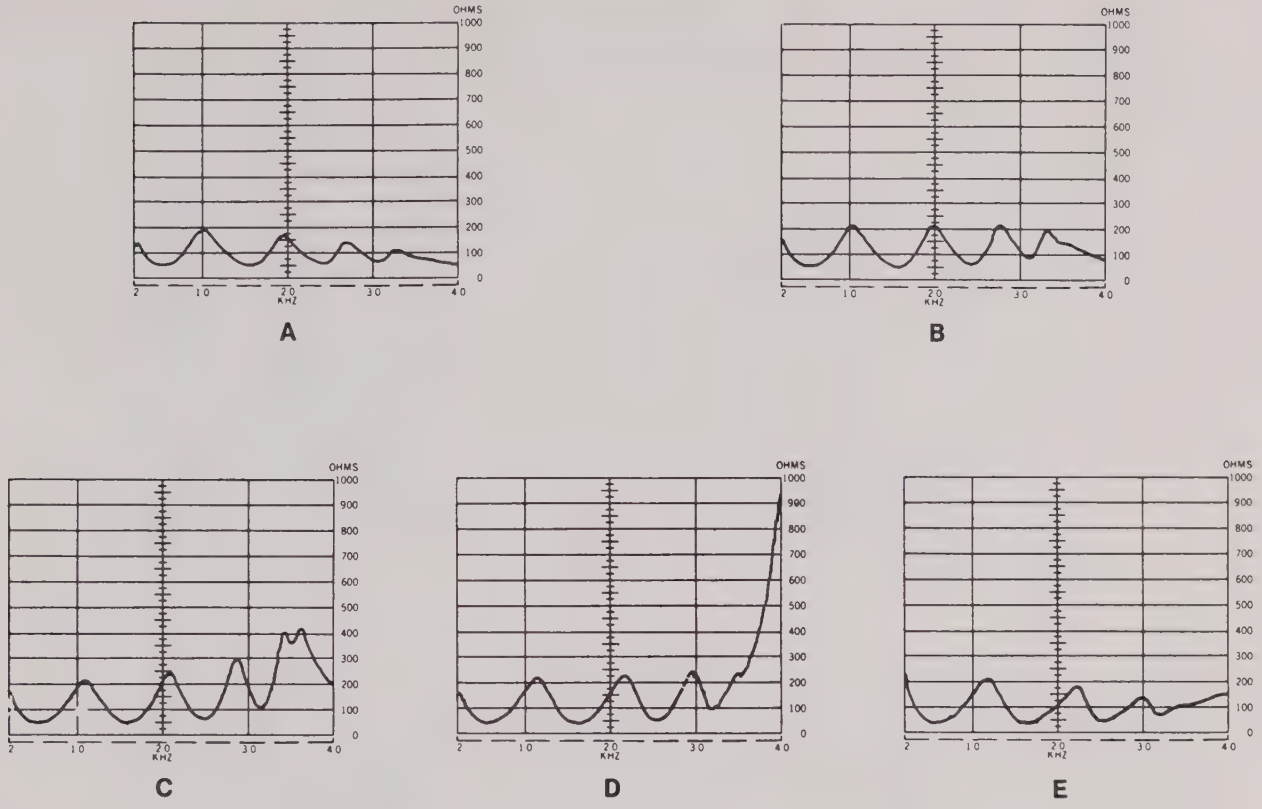


Figure 4—25. Effects Of Length Variations In CO End Section

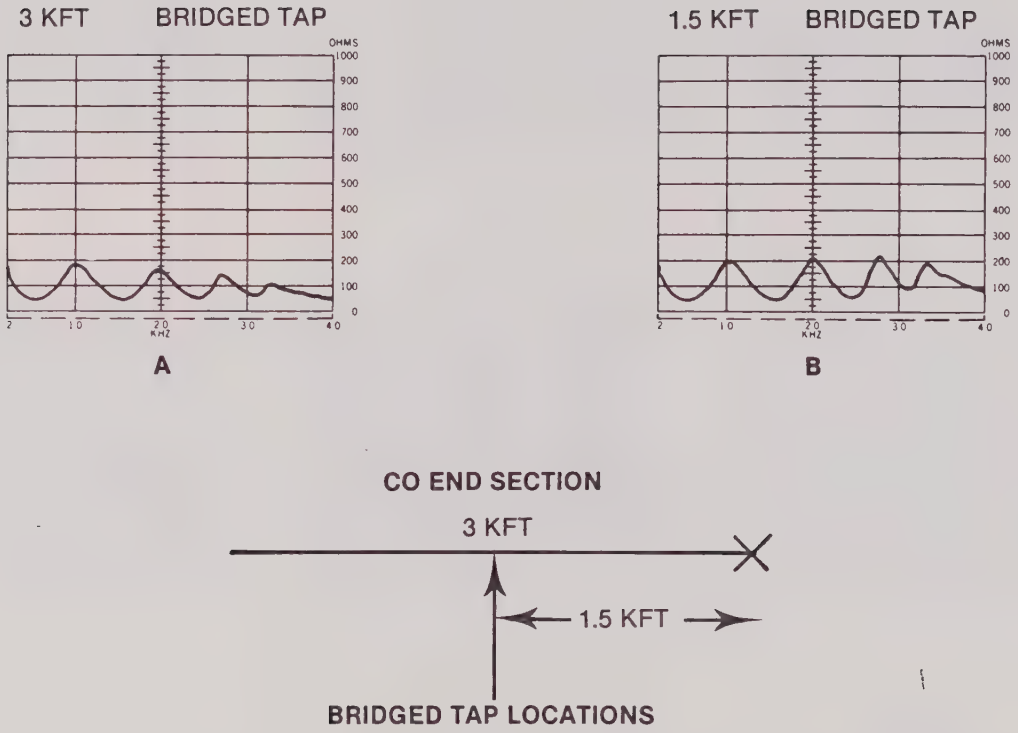


Figure 4—26. Effects Of Bridged Taps In CO End Section

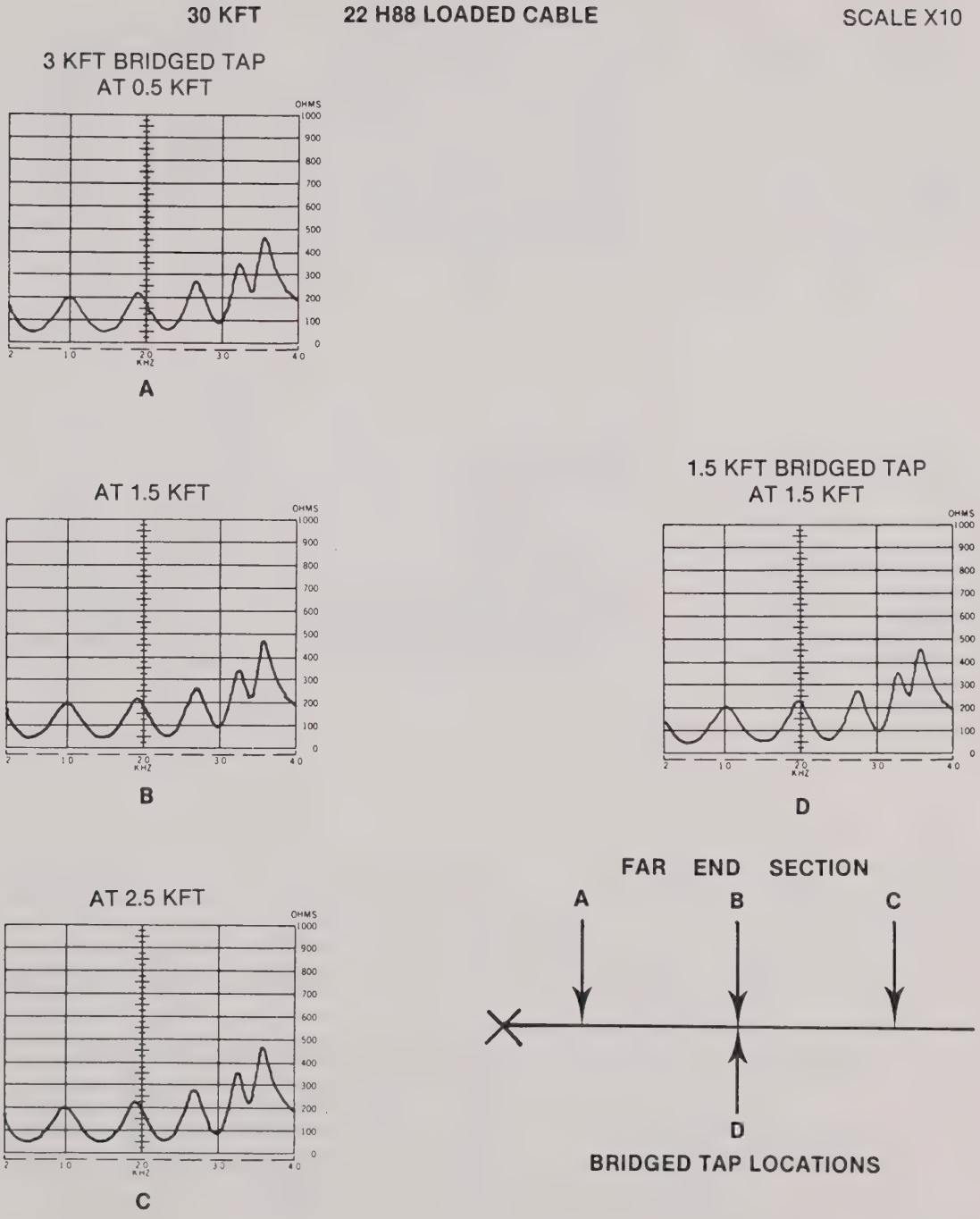
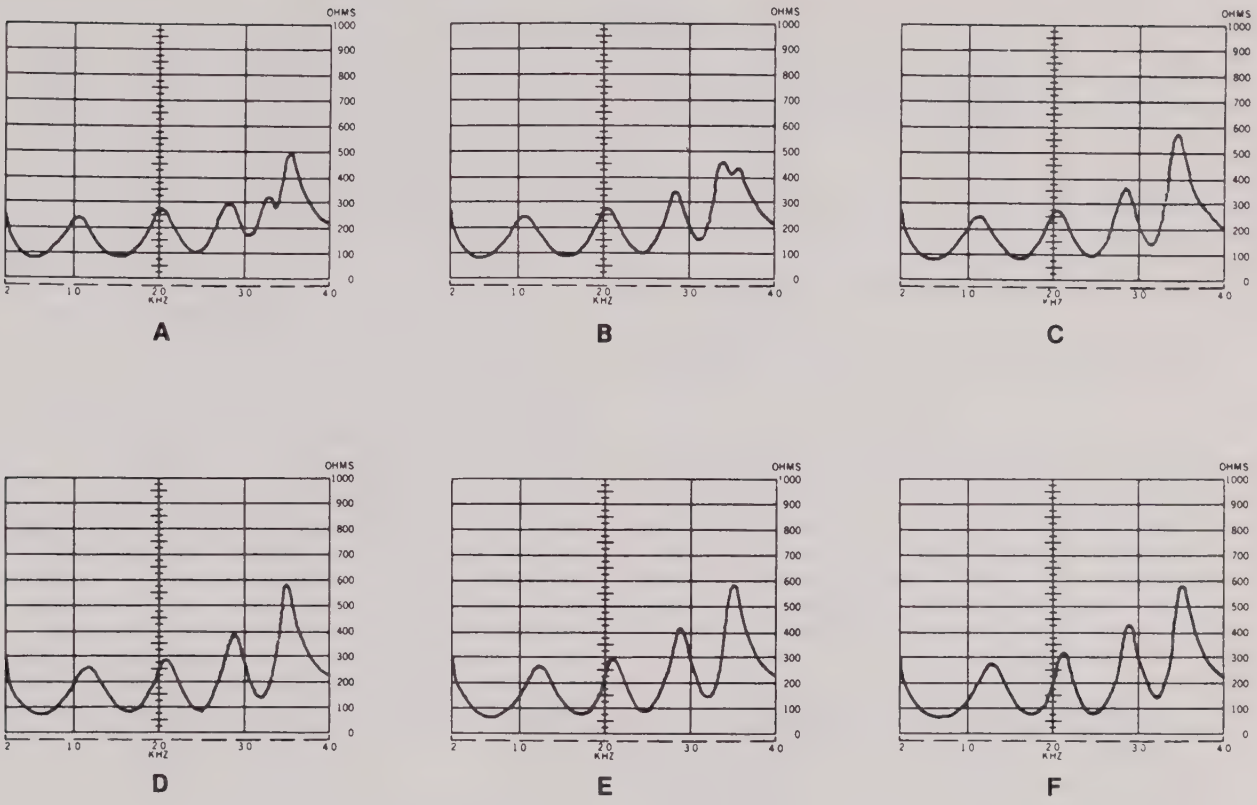


Figure 4—27. Effects Of Bridged Taps In Far End Section

24 TO 31.5 KFT 22H88 LOADED CABLE SCALE: X10



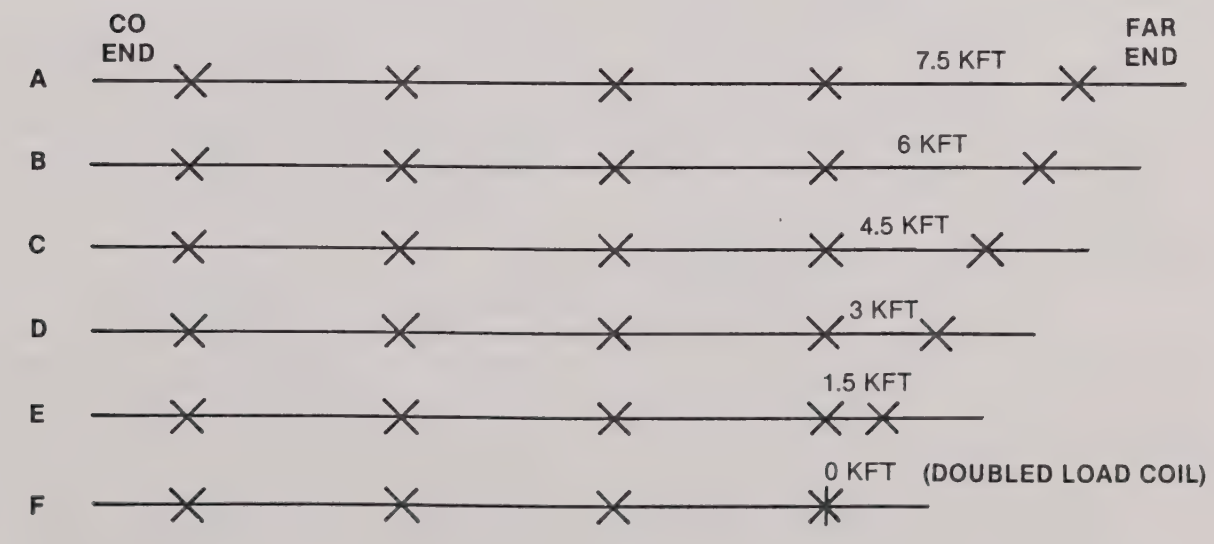


Figure 4—29. Effects Of Various Lengths In A Full Section Next To The Far End Section

SECTION 5

THEORY OF OPERATION

5.1 This section contains theory of operation and circuit descriptions for the Model 8100 Level Tracer. An overall description is first presented, at the block diagram level. Each major functional section of the Level Tracer is then described in detail for reference when calibrating or troubleshooting the unit.

5.2 OVERALL THEORY OF OPERATION

5.3 The Level Tracer overall functional design is shown in block diagram form in Figure 5−1. Primary signal flow paths are indicated by heavy weight lines. Medium weight lines show secondary signal flow paths. Control signal flow paths and power flow paths are designated by light weight lines. Figure 5−1 shows that the Level Tracer can be separated into transmit, input/output switching, receive, and power sections.

5.4 The **transmit section** generates and transmits test signal outputs. A test signal may be a tuned or swept frequency. A noise signal passed through an ERL weighted filter can also be selected as the test signal. All test signals go to the circuits under test via the LINE 1 and LINE 2 ports.

5.5 The **input/output switching section** controls signal flow and interfacing between the external world, the transmit section, and the receive section.

5.6 The **receive section** measures input signals received on the LINE 1 and LINE 2 ports. Measurement results may then be stored in a digital memory for display on a cathode ray tube. The test results for level, return loss, or impedance measurements are displayed as a function of frequency if the test signal is either a fixed or a swept frequency signal. Noise and ERL measurement results are displayed as horizontal lines on the CRT screen.

5.7 The receive section also measures the frequency of a test signal. This signal may either be the transmitted or the received test signal. The test signal frequency appears on a 4-digit display.

5.8 The **power section** contains the circuits which allow the Level Tracer to operate on an external ac voltage or on the dc voltage of its own internal, rechargeable batteries.

5.9 TRANSMIT SECTION OPERATIONS

5.10 Refer to Figure 5−1. The transmit section can generate a test signal with one of three characteristics. As determined by SIGNAL switch S2, the test signal may:

1. be manually tuned in frequency between 200 and 4000 Hz,

2. be a frequency swept from 200 to 4000 Hz, or

3. consist of noise passed through an ERL weighted filter.

5.11 In manual signal mode (tuned frequency signal), FREQ TUNING control R2 sets the signal frequency. In sweep signal mode, SWEEP SPEED switch S15 determines the sweep rate of the swept signal. In either manual or sweep signal mode, SF SUPP switch S1 forces the transmit section to skip a 300-Hz band centered about a frequency (factory set at 2600 Hz) controlled by SF SUPP ADJ potentiometer R4.

5.12 The test signal amplitude depends on the Level Tracer measurement mode chosen by FUNCTION test select switch S7. LEVEL dBm switches S3 and S4 control the test signal power **only** during level measurements. IMPEDANCE switch S5 changes the signal's voltage level to maintain the same power level into a 600- or a 900-ohm load.

5.13 The transmit section also performs some frequency processing. DISPLAY FREQUENCY switch S6 determines whether the send or the receive frequency will be processed. In the transmit section, the selected signal is shaped into a square wave and is routed to the receive section for eventual display on a digital readout. The selected signal is also changed into a dc signal with an amplitude proportional to the signal frequency. This dc signal is used by the receive section to update new data and to generate a frequency marker during frequency dependent measurements.

5.14 A more detailed description of the transmit section is presented in paragraph 5.39.

5.15 INPUT/OUTPUT SWITCHING OPERATIONS

5.16 The input/output switching section performs the following operations.

1. Controls the signal flow between the external world, the transmit section, and the receive section as determined by FUNCTION test select switch S7.

2. Bridges or terminates one of the two input ports as directed by INPUT switch S9.

3. Sets the Level Tracer input/output impedance at 600 or 900 ohms as directed by IMPEDANCE switch S5. A more detailed description of the input/output switching is presented in paragraph 5.72.

5.17 RECEIVE SECTION OPERATIONS

5.18 Refer to Figure 5—1. The receive section processes input signals for display on a cathode ray tube (CRT). The receive section provides two other outputs. One output consists of a frequency marker appearing on the CRT and the other output is the signal frequency seen on the DISPLAY FREQUENCY-Hz numeric display. As previously mentioned, the display frequency may be either the send or receive frequency.

5.19 The receive section can be divided into four major functions. These functions are:

1. analog signal processing,

2. digital signal processing,

3. video processing, and

4. frequency processing.

5.20 **Analog Signal Processing**

5.21 Analog signal processing consists of accepting a signal from the input/output switching section and producing a dc voltage proportional to the input signal strength. For impedance measurements, the dc voltage is linearly proportional, but for all other measurements the dc voltage is logarithmically proportional to the input signal.

5.22 A portion of the input signal is routed to the transmit section for frequency preprocessing.

5.23 A more detailed description of the analog signal processing is presented in paragraph 5.76.

5.24 **Digital Signal Processing**

5.25 During digital signal processing, the VERT IN signal from the analog signal processing circuit is converted into an 8-bit data word. Storage of this data word into a memory location occurs only if a trace memory switch is set at ACTIVE. Stored data is continuously strobed out of memory and reconverted into an analog signal. The reconverted signal is applied to the video processing circuit as the VERT deflection signal.

5.26 The F/V signal received from the transmit section has an amplitude proportional to the input signal frequency. During frequency-dependent measurements, this F/V signal determines the storage location of a newly converted data word. The F/V signal also generates a frequency marker sent to the video processing circuit.

5.27 The digital signal processing circuit also produces the HORIZ deflection signal which drives the video processing circuit. In addition, the digital signal processing circuit generates all timing and control signals necessary to process the VERTIN and F/V signals.

5.28 A more detailed description of the digital signal processing is presented in paragraph 5.98.

5.29 **Video Processing**

5.30 The video circuits generate all high voltages required to drive the cathode ray tube. The VERT and HORIZ deflection signals are amplified by differential amplifiers. The INTEN signal and MARKER pulse combine to control the voltage between the grid and the cathode.

5.31 A more detailed description of the video processing is presented in paragraph 5.132.

5.32 **Frequency Processing**

5.33 The frequency of the CNTR IN signal is doubled and then counted by a 4-digit frequency counter. The result is displayed on a 7-segment digital readout with leading zero blanking. The frequency processing has its own internal timing which provides a 2-Hz time base.

5.34 A more detailed description of the frequency processing is presented in paragraph 5.146.

5.35 POWER SECTION OPERATION

5.36 In ac operation, the power section changes an externally applied ac voltage into a +6.8 Vdc voltage. This dc voltage is then converted intol ± 15V and +5V regulated dc voltages which operate the Level Tracer. The +6.8 Vdc voltage also charges the internal batteries of the Level Tracer.

5.37 In battery operation, the battery voltage is converted into the required dc voltages. A meter circuit monitors the battery voltage and indicates the charge status of the batteries.

5.38 A more detailed description of the power section is presented in paragraph 5.160.

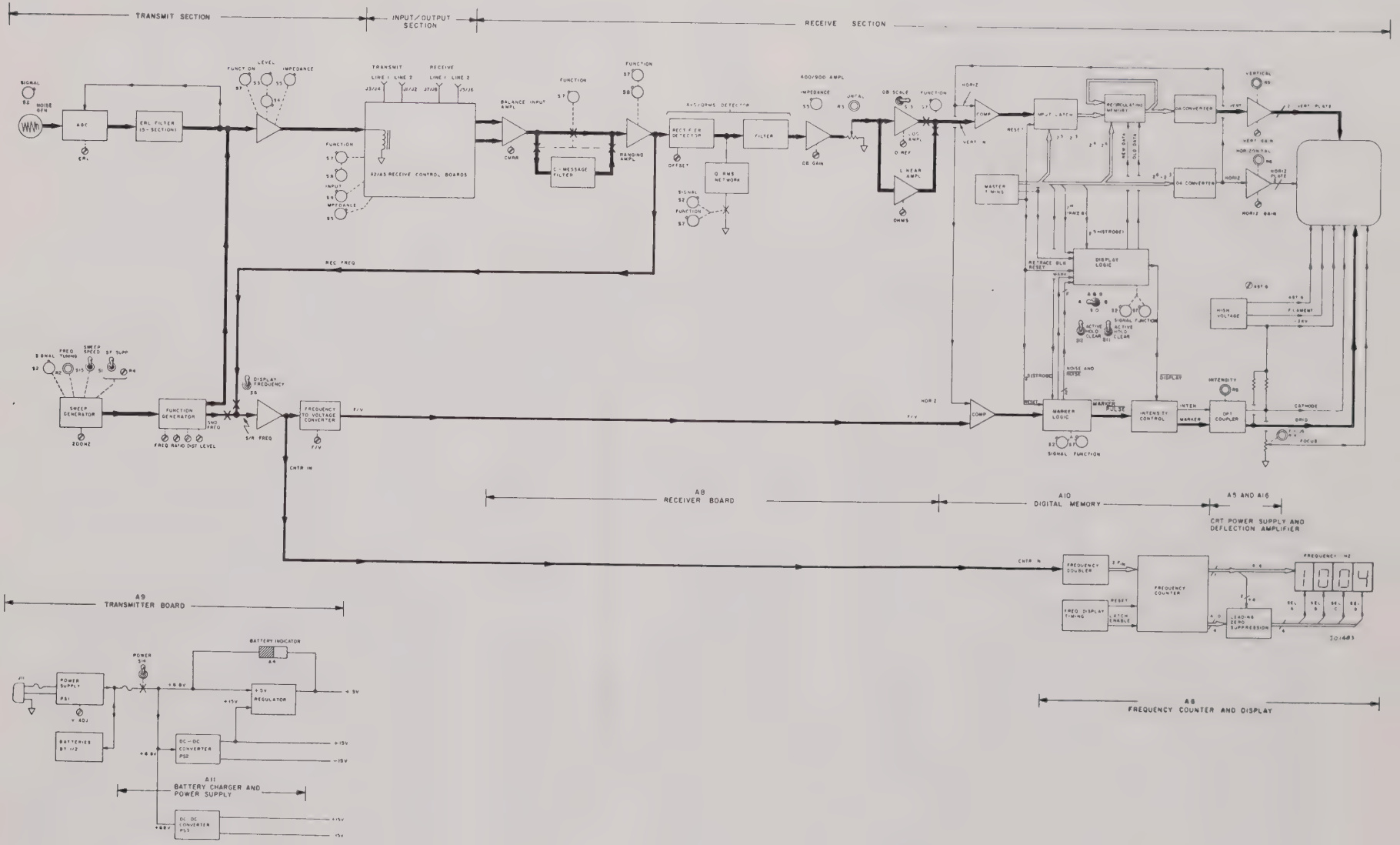
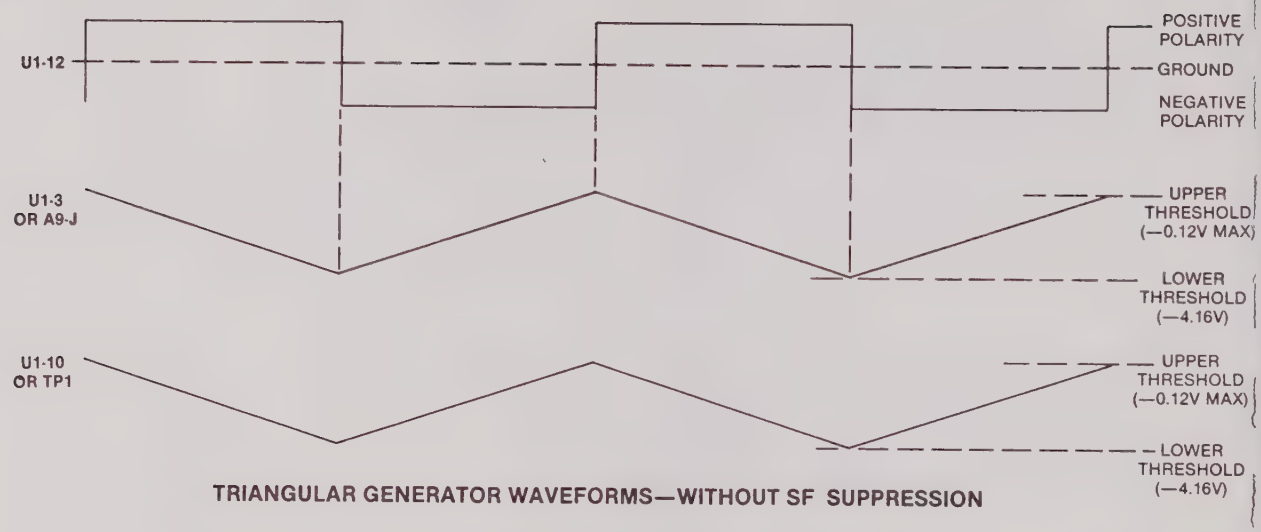
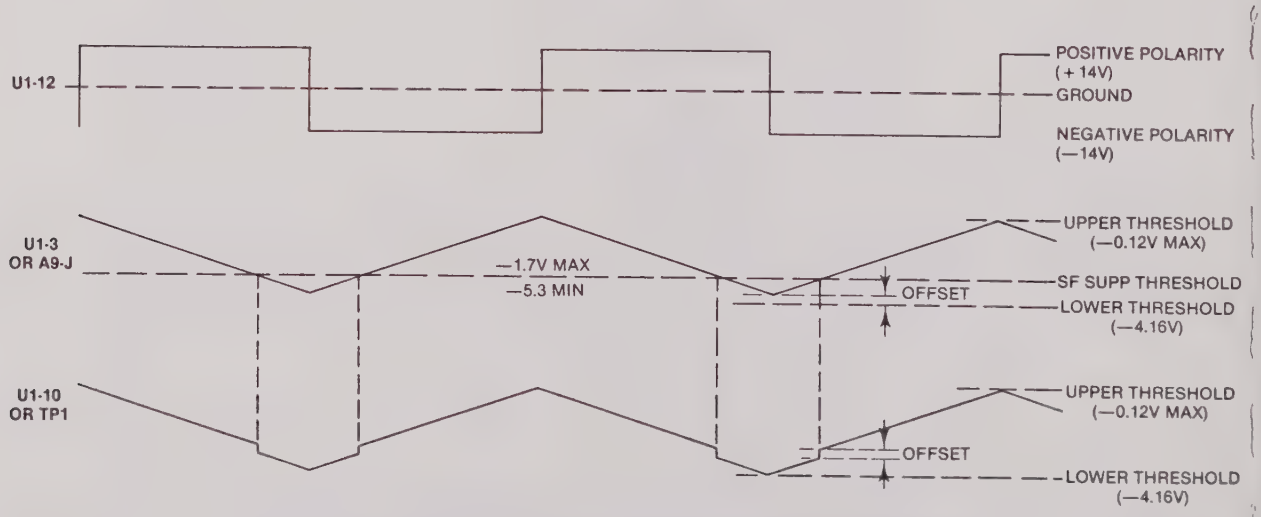


Figure 5—1. Level Tracer Functional Diagram



TRIANGULAR GENERATOR WAVEFORMS—WITHOUT SF SUPPRESSION



TRIANGULAR GENERATOR WAVEFORMS—WITH SF SUPPRESSION

C01516

Figure 5—2. Triangular Generator Waveforms

5.39 TRANSMIT SECTION, DETAILED DESCRIPTION

5.40 The transmit section generates and transmits test signals. Figure 7—22 is a detailed schematic diagram of the transmit section. Most of the circuit components, except for front panel controls and switches, are mounted on transmitter board A9. Figure 7—22 shows the interconnections between the controls, switches, and board.

5.41 The transmit section has a noise signal generator and a tuned/swept sine waveform generator. The setting of SIGNAL switch S2 enables only one of the generators to operate at a time. The output of the selected signal generator is amplified to a level controlled by the settings of FUNCTION switch S7, LEVEL dBm switches S3 and S4, and IMPEDANCE switch S5.

5.42 The square wave version of the sine wave generator output or a sample of the received signal (as selected by DISPLAY FREQUENCY switch S6) passes through a frequency preprocessing circuit.

5.43 NOISE GENERATOR

5.44 Wideband noise is obtained by the type of biasing on transistor Q2, contained within the feedback loop of amplifier U5B. The noise signal passes trhough a 5-stage bandpass filter and receives 30 dB of gain at 1 kHz. The filter consists of 1-pole lowpass stage U5A, two 2-pole highpass stages U4B and U4A, a 2-pole lowpass stage U4C, plus notch filter stage U4D. Figure 2—1 shows the ERL response (per Bell publication 41009) of the filter.

5.45 An automatic gain control (agc) loop holds the noise level variations down to 2-dB. The agc loop consists of peak detector U5C and integrating comparator U5D. ERL potentiometer R62 sets the reference level (430 mV maximum) appearing at the comparator input. The difference between the reference voltage and the peak detector output voltage (limited to a maximum of +0.7V by diode CR4) causes the comparator to increase or decrease the conductance of FET Q3. This change in conductance maintains the noise amplitude at a fairly constant level.

5.46 TUNED/SWEPT SINE WAVEFORM GENERATOR

5.47 The sine waveform generator shown in Figure 7—22 may be operated either as a manually tuned or a swept generator. In either mode, the waveform generator may be made to skip a 300-Hz band about a frequency set by SF SUPP switch S1.

5.48 Sweep Operation

5.49 With SIGNAL switch S2 set at SWEEP, comparator U1D, integrator U1A, and amplifier U1C comprise a triangular waveform generator. Comparator U1A has two thresholds (an upper threshold of −0.12V and a lower threshold of −4.2V) switched in by transistor Q1. Each time the voltage from the amplifier equals one of the threshold levels, the comparator changes its output voltage polarity and switches in the other threshold. The 200 Hz potentiometer R12 can adjust the upper threshold as far down as −0.55V.

5.50 Integrator U1A produces a ramp voltage with slope opposite to the polarity of the comparator output. That is, a negative-going ramp for a positive polarity and a positive-going ramp for a negative polarity.

5.51 The integrator time constant is set by resistors R25 and A1R3 together with capacitor C5. With SWEEP SPEED switch set at SLOW, both resistors are connected and the time constant equals 19 milliseconds, for a sweep time of 6 seconds. Placing the SWEEP SPEED switch at FAST bypasses resistor A1R3 to reduce the time constant by one-half, resulting in a 3-second sweep time.

5.52 The SWEEP SPEED switch may be also placed at RESET. Under this condition, the integrating capacitor is shorted out by resistor A1R4 and the output voltage is quickly driven toward the upper threshold level (lower frequency).

5.53 SF Suppression

5.54 When the SF SUPP switch is at OFF, the ramp voltage is always more positive than the voltage applied by the SF SUPP potentiometer R1. Therefore comparator U1B applies a −14V voltage to back bias diode CR1. This makes amplifier U1C operate as a voltage follower. Setting the SF SUPP switch at ON and adjusting the SF SUPP voltage to fall between the two thresholds causes the integrator ramp voltage to cross the SF SUPP threshold level once during each sweep.

5.55 When the ramp voltage is more negative than the sf supp threshold, comparator U1B applies +14V to forward-bias diode CR1. This results in a −250 mV offset voltage being added to the output of amplifier U1C. The offset voltage is removed when the ramp voltage becomes more positive than the sf supp threshold. Figure 5—2 shows the waveforms for the triangular generator with and without sf suppression. It is the abrupt change in output level which causes a frequency skip of 300 Hz.

5.56 Manually Tuned Operation

5.57 When SIGNAL switch S2 is set at MAN, comparator U1D is disconnected and integrator U1A is reconfigured as an inverting attenuator with 10.8 dB to 11.5 dB loss. FREQ TUNING control R2 applies a tuning voltage between 0V and +15V to the attenuator. Therefore, this tuning voltage appears at the amplifier output as a voltage between 0V and −4.3V. Resistor R6 causes a minus 100-mV offset to be added to the attenuator output. The offset ensures that the frequency does not fall below 150 Hz. This tuning voltage range (−0.1V to −4.4V) has the same nominal range as the triangular sweep waveform. FREQ TUNING control R2 is a dual potentiometer with a coarse tune section and a fine tune section. The coarse tune section has a 15-volt adjustment range while the fine section can change the coarse setting by ±4%.

5.58 The SF SUPP switch has the same effect on the manually tuned operation as it has on the swept operation. That is, an offset voltage of −250 mV is added to the amplifier output when the attenuator output is more negative than the sf supp threshold.

5.59 Waveform Generator

5.60 In either tuned or swept mode, the voltage output of amplifier U1C controls function generator U3. The function generator produces a sine waveform and a square waveform with frequencies directly proportional to the input voltage.

5.61 Three adjustments are present on the function generator. FREQ ADJ potentiometer R14 sets the frequency constant of proportionality at 1000 Hz/volt. RATIO ADJ potentiometer R13 places the duty cycle of the square waveform output at 50%. The third adjustment operates in conjunction with distortion detector U2. Initially DIST ADJ potentiometer R16 is set for minimum distortion at 2000 Hz. Then distortion detector U2 automatically corrects the function generator output for all other frequencies.

5.62 The waveform present at TP2 is a sine waveform superimposed on a $-V_A/2$ dc level and capacitor C9 is essentially an ac short (compared to 100 kohms) in the frequency range of interest. For undistorted sine waveforms, the distortion detector sees equal dc levels at both its inputs. The distortion detector returns a $-V_A/2$ level to the function generator via potentiometer R16. The dc component of a distorted waveform unbalances the input dc levels. This causes the distortion detector to add to or subtract from the $-V_A/2$ voltage an amount proportional to the error voltage. The error voltage causes the function generator to reduce the distortion present on the sine waveform.

5.63 Note that the tuned/swept sine waveform generator does not operate when SIGNAL switch S2 is set at ERL since this disconnects the dc voltages from the sine waveform generator.

5.64 Output Level Control

5.65 The sine or noise signal is amplified to its final output level by cascaded amplifiers U8A and U8B. The feedback provided by resistor R116 and capacitor C48 removes any dc component present on the output signal due to amplifier offsets.

5.66 Table 5−1 shows the gains for the various positions of FUNCTION switch S7 and the effects of LEVEL dBm switches S3 and S4. IMPEDANCE switch S5 changes the gain of amplifier U8B by 1.76 dB. Since the receive section automatically normalizes the input signal to a 600-ohm signal, no change is observed and no error occurs during impedance and return loss measurements regardless of IMPEDANCE switch position. During noise measurements, the transmit section is of course not connected to the circuit under test.

5.67 Note in Table 5−1 that the gain for an ERL signal is 19.6 dB higher then for a sine wave signal since the initial noise source output level is lower than the sine wave generator output level. The actual difference between the gains can vary by ±0.8 dB. During calibration the sine wave signal gain is adjusted (using LEVEL potentiometer R77) to obtain 0 dBm for LEVEL dBm switch settings of 0 and 0. The ERL noise signal is later adjusted via ERL potentiometer R62 to obtain an average of 0 dBm for the same LEVEL dBm switch settings. The amplified signal goes to input/output board A2 as the XMOUT signal.

5.68 Frequency Preprocessing

5.69 FREQUENCY DISPLAY switch S6 selects either the square wave output of function generator U3 or a sample of the received signal as the input for frequency preprocessing. Frequency preprocessing is a two-step operation. The first step shapes the signal into a square wave with logic levels of +5V and 0V. The second step produces a dc voltage proportional to the input frequency

5.70 The wave shaping is done by comparator U6B and level translator Q5. The comparator is a level detector circuit with ±14 mV trip points. This comparator has a very high gain (open loop gain) for low level to provide fast switching signals but is limited to a gain of 100 for higher input levels. Transistor Q5 translates the ±14 V levels out of the comparator to +5 V and 0 V levels respectively. A portion of the shaped signal goes to frequency counter A6 and the other portion passes on to the frequency-to-voltage conversion circuit.

5.71 The frequency-to-voltage converter consists of differentiator Q4, timer U7, and lowpass filter U6A. The differentiating circuit produces a negative pulse on each cycle of the input signal (either the send or the receive frequency). Each pulse triggers the timer to produce a 93-microsecond positive pulse. As the input frequency increases so does the duty cycle of the timer output. Therefore the dc component level increases as the duty cycle becomes larger. Three-pole lowpass filter U6A (with a 54 Hz frequency cut-off) passes only the dc component into memory board A10. F/V potentiometer R63 is normally adjusted to obtain +4.9 V for a 4-kHz input frequency.

5.72 INPUT/OUTPUT SWITCHING, DETAILED DESCRIPTION

5.73 The input/output switching section configures the Level Tracer for each type of measurement. Table 5—2 summarizes the input/output switching operation and Figures 5—3 through 5—7 show the detailed configuration diagrams for each measurement.

5.74 RECEIVE SECTION, DETAILED DESCRIPTION

5.75 The receive section processes input signals. The detailed description of the receive section is separated into four parts. These parts are arranged as follows:

1. Analog signal processing description, paragraph 5.76

2. Digital signal processing description, paragraph 5.98.

3. Video processing description, paragraph 5.132.

4. Frequency processing, paragraph 5.146.

5.76 RECEIVE SECTION, ANALOG SIGNAL PROCESSING DESCRIPTION

5.77 The analog signal processing circuits accept an input signal from the input/output switching section and provide a dc level to the digital signal processing circuits. The dc level is logarithmically proportional to the input signal except for "impedance" measurement. During an "impedance" measurement the analog processing circuits supply a dc level linearly proportional to the input signal. Figure 7—20 is a detailed schematic diagram of receiver board A8 which contains most of the analog processing circuits. Figure 7—20 includes the interconnections between the receiver board and the front panel controls and switches.

5.78 Balanced Input Amplifier

5.79 The input signal is changed from a balanced signal to an unbalanced signal by high-impedance, balanced amplifier U2A/U2B. CMRR ADJ potentiometer R5 adjusts the gain of U2A to precisely balance both inputs and produce a high common mode rejection ratio. During "level", "impedance", and "rl" measurements the output of the balanced amplifier goes directly to ranging amplifier U2C. For a "noise" or a "noise/gnd" measurement the balanced amplifier output passes through a C-message filter before reaching the ranging amplifier.

5.80 C-Message Filter

5.81 The C-message filter consists of four active filter stages U1A through U1D. The C-message filter has an overall gain of 30 dB at 1kHz with the last stage adjusted during final test. Figure 2—2 shows the filter response curve.

5.82 Ranging Amplifier

5.83 Ranging amplifier U2C is a multiple gain amplifier with a nominal gain of 35.5 dB when FUNCTION range select switch S8 is set at —30. The gain decreases in 10-dB steps as the FUNCTION range select switch travels from —30 to 10 during a "level" measurement. Gain reduction is achieved by a transistor switching a resistor in parallel with resistor R34.

5.84 The ranging amplifier gain changes in a similar manner for "noise", "noise/gnd", and "rl" measurements. During an "impedance" measurement, transistor Q8 maintains the ranging amplifier gain at 35.5 dB for all positions of the FUNCTION range select switch. After range amplification the signal goes to the average/Q-rms detector circuit. A portion of the signal also goes to the transmit section for frequency preprocessing (refer to paragraph 5.68).

5.85 Average/Q-rms Detector

5.86 The average/Q-rms detector consists of full-wave rectifier U2D/U3A and filter/amplifiers U3B/U3C. Full-wave rectification is accomplished by algebraically adding a sine waveform to the half-wave rectified sine waveform output of precision rectifier U2D. The gain supplied by summing amplifier U3A is twice as large for the half-wave rectified sine waveform as it is for the sine waveform. Thus, the output of summing amplifier U4D is a full-wave rectified waveform as shown in Figure 5—8. The base-emitter junctions (diodes) of Q10 are required for Q-rms detection. OFFSET potentiometer R50 reduces the dc offsets to attain a 40 dB dynamic range.

Table 5—1. Output Level Gain

FUNCTION	AMPLIFIER U8A	AMPLIFIER U8B
LEVEL		
SIGNAL switch S2 at MAN or SWEEP, IMPEDANCE switch S5 at 900.	−4.8±0.8 dB for LEVEL dBm switch S3 at 10. Output level decreases in 10-dB steps as LEVEL dBm switch S3 moves from 10 to −20.	+9.6 dB for LEVEL dBm switch S4 at −9. Output level increases in 1-dB steps as LEVEL dBm switch S4 moves from −9 to 0.
SIGNAL switch S2 at ERL, IMPEDANCE switch S5 at 900.	+14.8 dB for LEVEL dBm switch S3 (19.6 dB more than for sine waveform). Output level decreases in 10-dB steps as LEVEL dBm switch S3 moves from 10 to −20.	+9.6 dB. Output level increases in 1-dB steps at LEVEL dBm switch S4 moves from −9 to 0.
IMPEDANCE		
SIGNAL switch S2 at MAN or SWEEP, IMPEDANCE switch S5 at 900.	−14.8 dB (10 dB less than LEVEL position). LEVEL dBm switch S3 inoperative.	+12.6 dB. LEVEL dBm switch S4 inoperative.
NOISE or NOISE/GND		
SIGNAL switch S2 at MAN or SWEEP, IMPEDANCE switch S5 at 900.	Less than −54.8 dB (50 dB less than LEVEL position). LEVEL dBm switch S3 inoperative.	9.6 dB. LEVEL dBm switch S4 inoperative.
RL		
SIGNAL switch S2 at MAN or SWEEP, IMPEDANCE switch S5 at 900.	−21.9 dB (17.1 dB less than LEVEL position). LEVEL dBm switch S3 inoperative.	9.6 dB LEVEL dBm switch S4 inoperative.
SIGNAL switch S2 at ERL, IMPEDANCE switch S5 at 900.	−2.3 dB (19.6 dB more than for a sine waveform). LEVEL dBm switch S3 inoperative.	9.6 dB. LEVEL dBm switch S4 inoperative.

5.87 When the input signal is not a noise signal, the full-wave rectified signal goes to lowpass filters U3B and U3C. The filters allow only the dc component to pass. Therefore, the rectifier and the filters combine to form an average detector.

5.88 For a noise signal (FUNCTION switch S7 set at NOISE or NOISE/GND or SIGNAL switch S2 set at ERL) base-emitter junction 2-3 of Q10, capacitor C19, plus resistors R54, R55, and R84 form a weighting network. The base-emitter junction 6—5 of Q10 compensates for the drop of the other base-emitter junction. The weighting network has properties such that sine waves and white noise of equal power produce the same level at the output of filter stage U3B.

5.89 In this circuit, the detected level for a sine wave input lies between the average and the peak values. Therefore, this type of detector is called quasi-rms (or q-rms)since the rms value of a sine wave also falls between the average and the peak values.

5.90 DB GAIN potentiometer R58 at the input to filter U3C sets the overall gain for the receiver board. IMPEDANCE switch S5 reduces the gain of filter U3C by 1.76 dB when set at 900. This action normalizes a 900-ohm signal into a 600-ohm signal. This means that signals with equal powers across a 900-ohm load and a 600-ohm load produce the same voltage levels at the output of filter U3C.

FUNCTION Test Select Switch S7 Position	Configuration Diagram	Description Of Input/Output Switching	FUNCTION Range Select Switch S8	INPUT Switch S9	IMPEDANCE Switch S5
LEVEL	Figure 5–3	Configures the Level Tracer as an instrument capable of transmitting and receiving test signals independently. Routes test signal to output ports. Routes input signal from **one** input port to receive section.	Switch has no direct effect on input/output switching	Selects the input port and terminates or bridges the input port.	Sets the output impedance and the input termination at 600 or 900 ohms
IMPEDANCE	Figure 5–4	Configures the Level Tracer as a constant current source. The current source appears at the receive input ports and the receive section measures the resulting voltage across **one** of the input ports.	Selects the constant current value. This chooses the impedance range.	Selects the input port.	Switch has no direct effects on input/output switching.
NOISE	Figure 5–5	Configures the Level Tracer as a circuit noise measuring instrument. Receive section measures the noise present across the tip and ring of the circuit under test.	Switch has no direct effect on input/output switching.	Selects the input port and terminates or bridges the input port.	Sets the input termination at 600 or 900 ohms.
NOISE/GND	Figure 5–6	Configures the Level Tracer as a longitudinal noise measuring instrument. Receive section measures the average tip/ring noise to ground attenuated by a 40-dB pad.	Switch has no direct effect on input/output switching.	Selects the input port	Sets the input termination at 600 or 900 ohms.
RL	Figure 5–7	Configures the Level Tracer as a bridge-type instrument.	Switch has no direct effect on input/output switching.	Switch has no direct effect on input/output switching.	Switch has no direct effect on input/output switching.

Table 5–2. Input/Output Switching Configurations

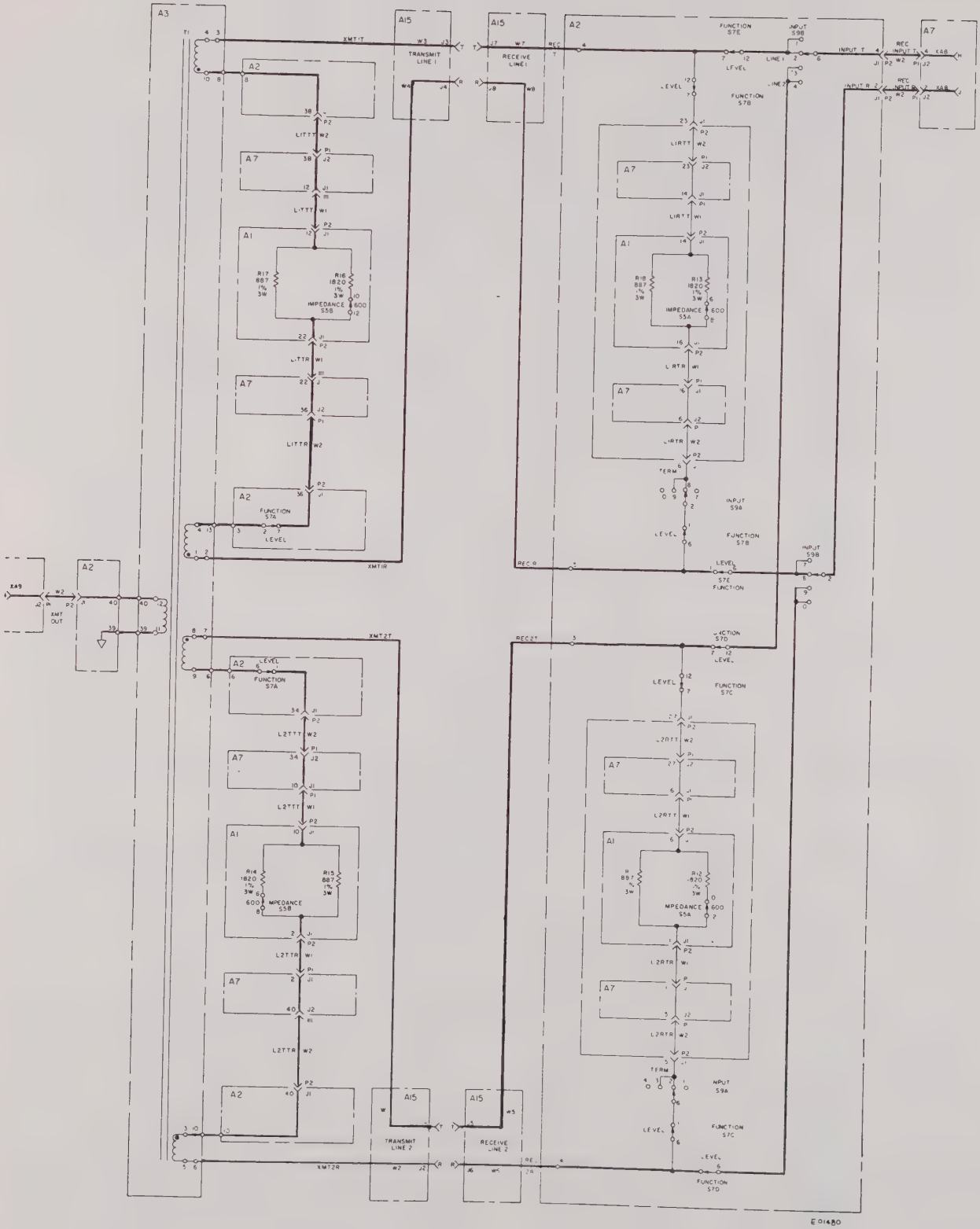


Figure 5—3. Input/Output Configuration For "Level" Measurements.

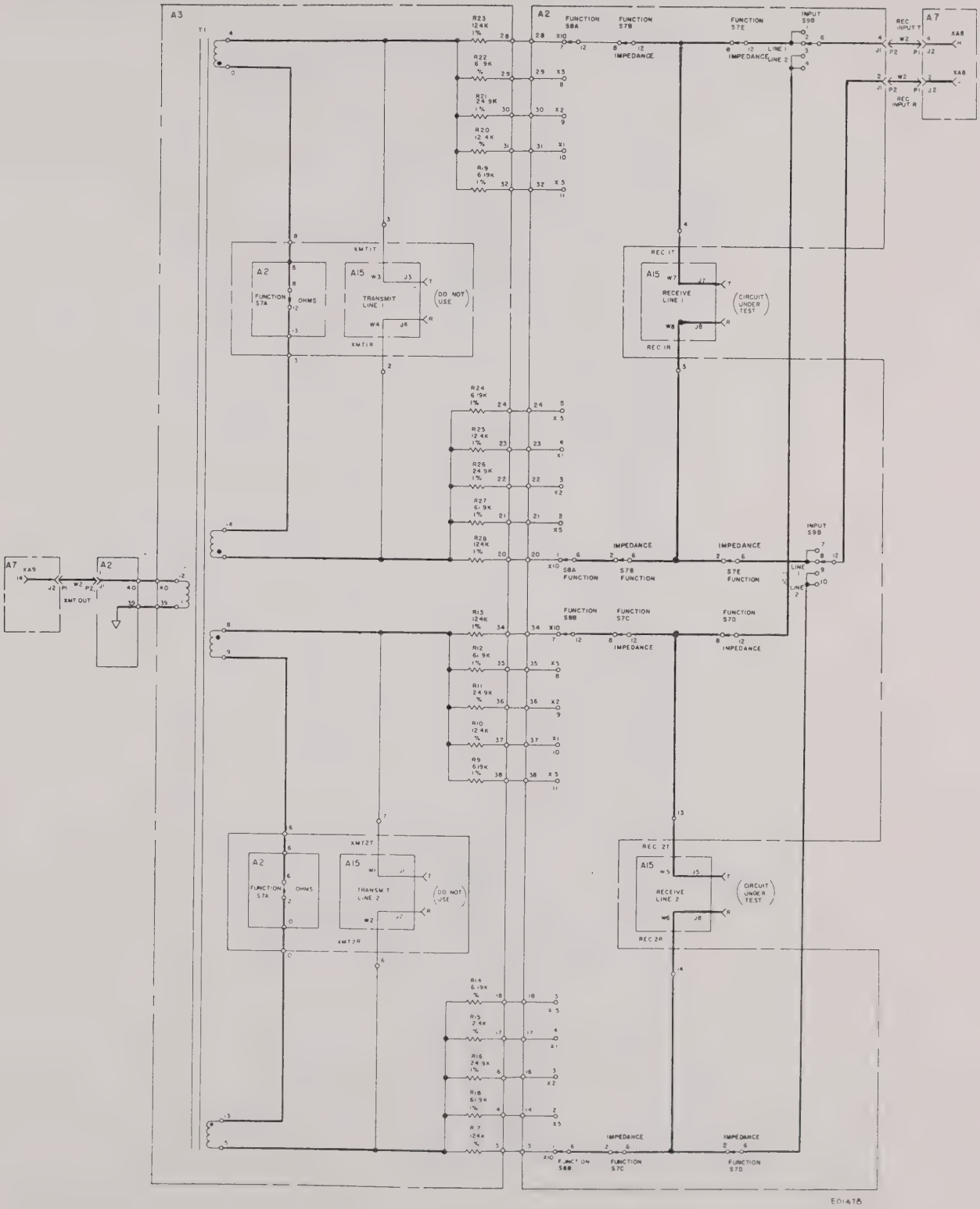


Figure 5—4. Input/Output Configuration For "Impedance" Measurements.

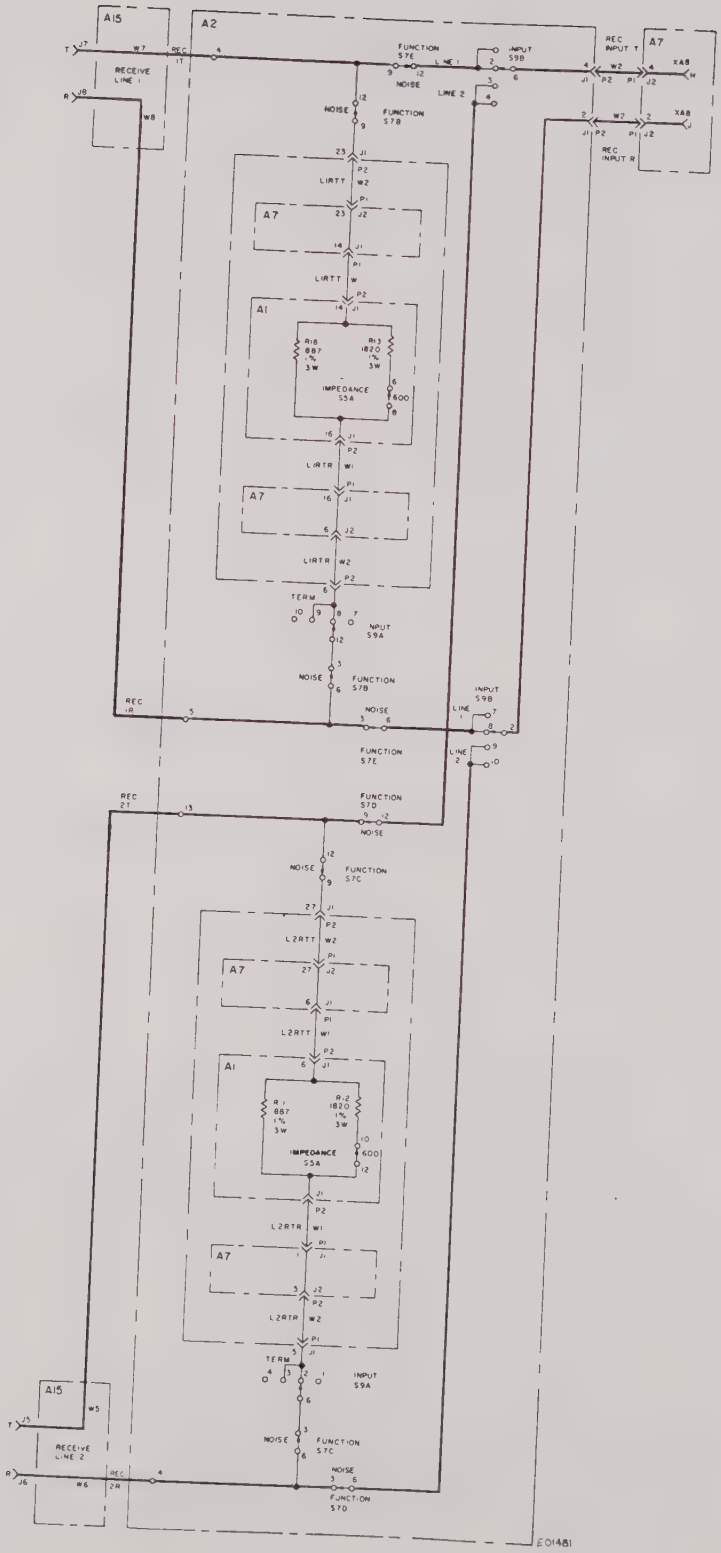


Figure 5—5. Input/Output Configuration For "Noise" Measurement

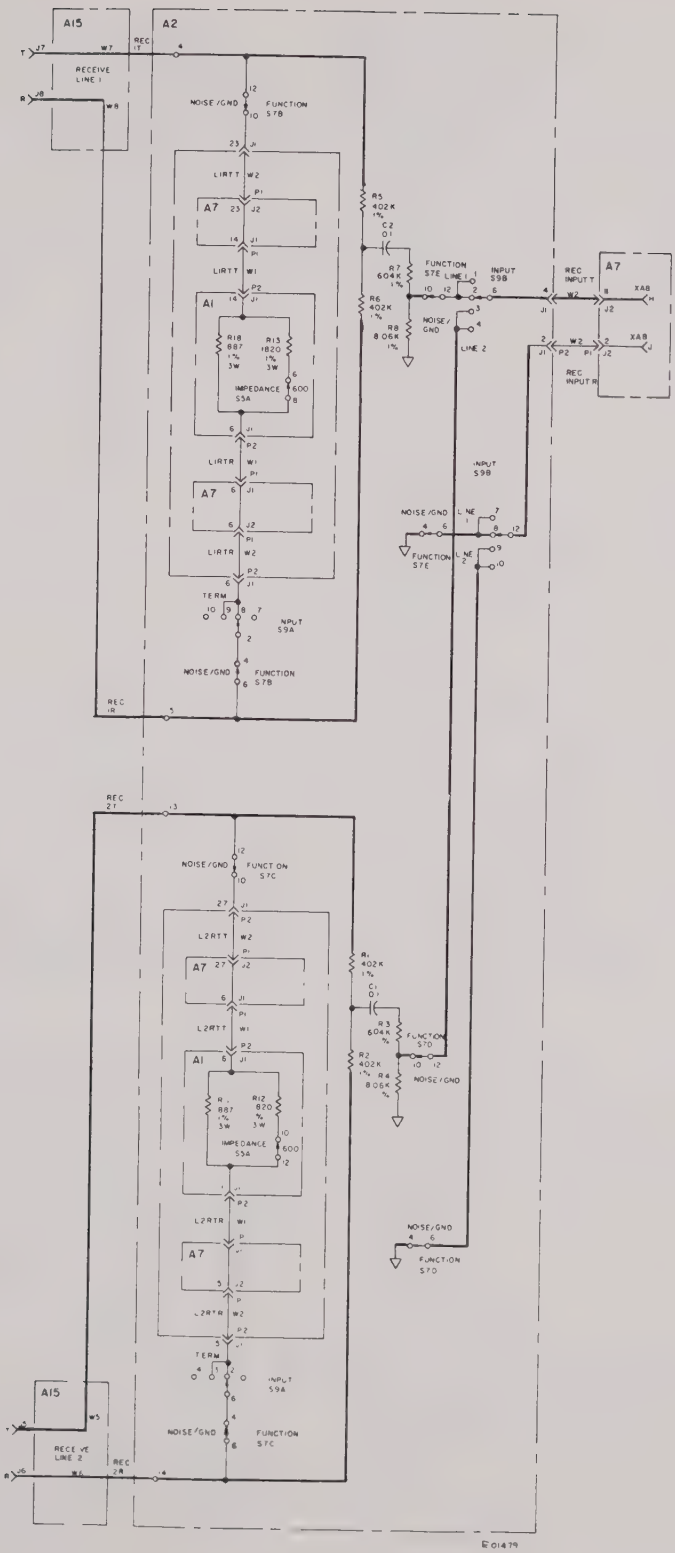


Figure 5—6. Input/Output Configuration For "Noise/Gnd" Measurements.

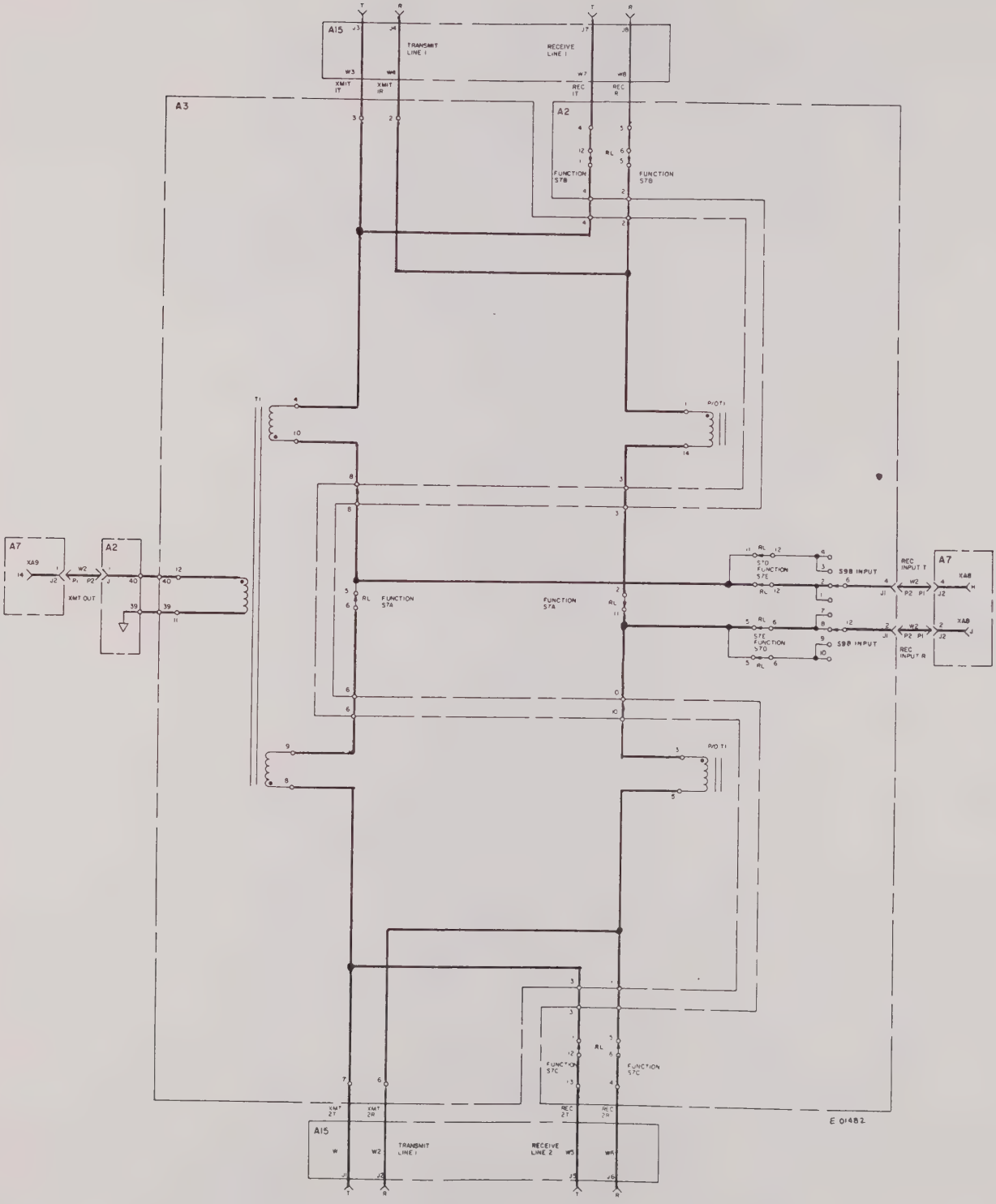


Figure 5—7. Input/Output Configuration For "RL" Measurements.

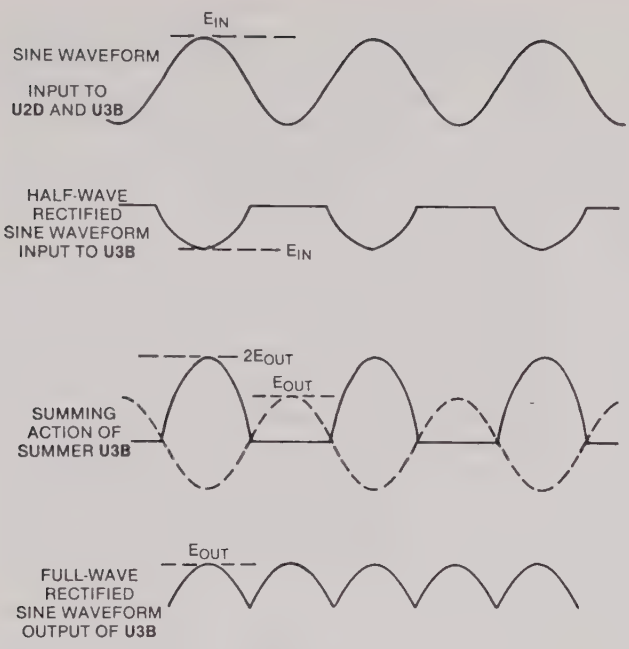


Figure 5—8. Full-Wave Rectification

5.91 All or some of the normalized detected signal goes to log amplifier U4/U5A and then to scale amplifier U5B in all measurement modes (except "impedance" measurements). During an "impedance" measurement, the normalized detected signal goes to linear amplifier U3D.

5.92 UNCAL control S16/R31 determines the level of detected signal that reaches the next stage. Normally, the UNCAL control is at off, and all of the detected signal goes on to the next stage. When set at on, the UNCAL control can reduce the level of the detected signal reaching the next stage by as much as 9.5 dB. This feature is useful in separating two nearly identical traces on the CRT or in positioning a specific frequency on the 0 dB reference graticule line.

5.93 Log Amplifier And Scale Amplifier

5.94 Log amplifier U4/U5A produces an output voltage proportional to the logarithm of its input voltage. The log amplifier transfer function is such that an input of 2V produces an output of 0 V and that a +10-dB change in the input voltage appears as a 1-volt change on the output voltage. Note that a 2V input at the log amplifier represents an input level of +10 dBm, 0 dBm, −10 dBm, −20 dBm, or −30 dBm as determined by FUNCTION range select switch S8 for a level measurement.

5.95 Scale amplifier U5B normally inverts and amplifies the log level by 1.16 and adds a dc offset of at least 3.7 volts. The offset voltage, adjusted by 0 REF potentiometer R74, separates the 0-dB and "clear" traces. by 32 dB or more. DB SCALE switch S13, when set at X¼, increases the scale amplifier gain by a factor of 4 without affecting the offset voltage. Thus, all displayed signals from 2 dB above to 8 dB below the 0-dB reference line are magnified by a factor 4. Signals beyond this range go off the screen. Note that a 4-dB variation on the display screen should be interpreted as a 1-dB variation when the DB SCALE switch is set at X¼.

5.96 Linear Amplifier

5.97 Linear amplifier U3D accepts the detected signal and passes the signal on to the memory board via the FUNCTION switch. OHMS potentiometer R64 adjusts the full scale gain for "impedance" measurements. FUNCTION test select switch S7 chooses either the log signal or the linear signal for digital processing by the memory board.

5.98 RECEIVE SECTION DIGITAL SIGNAL PROCESSING DESCRIPTION

5.99 The digital signal processing circuits receive the VERT IN signal from the analog signal processing circuits and the F/V signal from the transmit section. Recall that the amplitude of VERT IN is proportional to log of the input signal level except during an "impedance" measurement. For "impedance" measurements, VERT IN is linearly proportional to the input signal level. The amplitude of F/V is linearly proportional to the input signal **frequency.**

5.100 Refer to paragraph 5.24 for a brief discussion of the digital processing circuits. Figure 7—24 is a detailed schematic diagram of the digital memory board A10 which contains most of the digital processing circuits. Figure 7—24 includes the interconnections between the digital memory board and the front panel switches.

5.101 Master Timing

5.102 Operation of the digital signal processing is controlled by a timing circuit which generates all clock signals used within the memory board. See Figure 5—9A for pertinent waveforms of the timing control circuit.

5.103 Nand-gates U4A,D and crystal Y1 form a gated, crystal-controlled oscillator. The clock signal, buffered by gate U4C, runs at 1.544 MHz. Fourteen-bit binary counter U6 divides this time base clock into 11 timing signals (bits 2^4 through bits 2^{14}). The high-to-low transition of bit 2^{13} triggers one-shot U4B/U4A via buffer

U2D. The 0.7-millisecond pulse from the one-shot performs three basic functions:

a. Inhibits the oscillator, thus holding the count of U6 at 0 or 2^{14}. As soon as the one-shot pulse ends, all timing operations resume.

b. Provides reset pulse for the input logic circuits.

c. Provides a blanking pulse for horizontal retrace on the CRT screen.

5.104 The timing signals from counter U6 perform the following functions.

a. Bit 2^5 controls the strobing of VERT IN and F/V signals.

b. Bits 2^4-2^6 control data shifting through the memory.

c. Bits 2^6-2^{13} form an 8-bit word which relates the horizontal sweep voltage with the memory address location.

c. Bit 2^{14} selects the trace to be refreshed.

5.105 **Horizontal Sweep**

5.106 D/A converter U8/U10A accepts the input word formed by bits 2^6-2^{13} and produces a ramp voltage. The ramp starts at zero volts when the input word is zero and increases negatively toward −5.0 V as the input word increases (see Figure 5−9A). The HORIZ ramp voltage drives the horizontal deflection amplifier. The HORIZ ramp voltage also assists in the processing: (1) of the VERT IN signal by the vertical comparator and input latch circuits, and (2) of the F/V signal by the f/v comparator and marker logic circuits.

5.107 **F/V Comparator And Marker Logic**

5.108 The F/V comparator and marker logic circuits monitor the F/V signal with the HORIZ ramp voltage to produce a MARK signal and a $\overline{\text{MARKER PULSE}}$. The MARK signal is used by the display logic to generate control signals for writing data into a trace memory. The $\overline{\text{MARKER PULSE}}$ is used by the intensity control circuit. See Figure 5−9E for pertinent timing waveforms of the marker logic.

5.109 Comparator U10C monitors the F/V signal together with the HORIZ ramp voltage. When the absolute value of HORIZ exceeds the F/V level a logic one is applied to the marker logic circuit. At this time, the value of the address word (formed by bits 2^6-2^{13}) equals the amplitude of HORIZ which, in turn, equals the amplitude of F/V. Recall that F/V is linearly proportional to the input signal frequency.

5.110 The next strobe (bit 2^5) causes flip-flops U24A, B, gates 16D, and drivers U25C,F to produce a MARK pulse. Normally, both flip-flops remain set until the next RESET period. Therefore only one MARK pulse occurs during each horizontal sweep. The MARK pulse passes through gate U16B and buffer U2E to appear as $\overline{\text{MARKER PULSE}}$ only during frequency dependent (non-noise type) mesurements. (FUNCTION test select switch set at LEVEL, IMPEDANCE, or RL and SIGNAL switch set at MAN or SWEEP). Similarly, the display logic uses the MARK pulse only during non-noise type measurements.

5.111 Recall that a test signal sweep rate may be either slow (6 seconds) or fast (3 seconds) while the HORIZ ramp has a 6-millisecond repetition period. Thus, 1000 MARK pulses for a slow sweep or 500 MARK pulses for a fast sweep occur during each test signal sweep. This means that each trace memory may be updated 500 times (slow sweep) or 250 times (fast sweep) during each test signal sweep since the trace memories are alternately updated. The display control determines whether or not to update a trace memory.

5.112 **Display Logic**

5.113 The display logic circuit monitors the states of the DISPLAY switches and produces signals to control the data input into a recirculating memory and to blank out the display screen when necessary.

5.114 And-or gates U19A,C together with associated gates and inverters monitor the A and B display switches to generate the NEW DATA and OLD DATA control signals. Table 5−3 summarizes the results for the various positions of A and B display switches.

5.115 And-or gate U19B and inverter U25E monitor the A&B trace select switch to produce the $\overline{\text{DISPLAY}}$ control signal. A high $\overline{\text{DISPLAY}}$ causes blanking to the display screen. Figure 5−9D shows that blanking occurs during the reset period. Blanking also occurs during the horizontal sweep time of a trace if that trace was not selected to be displayed. Blanking of the display screen occurs via the intensity control cirucit.

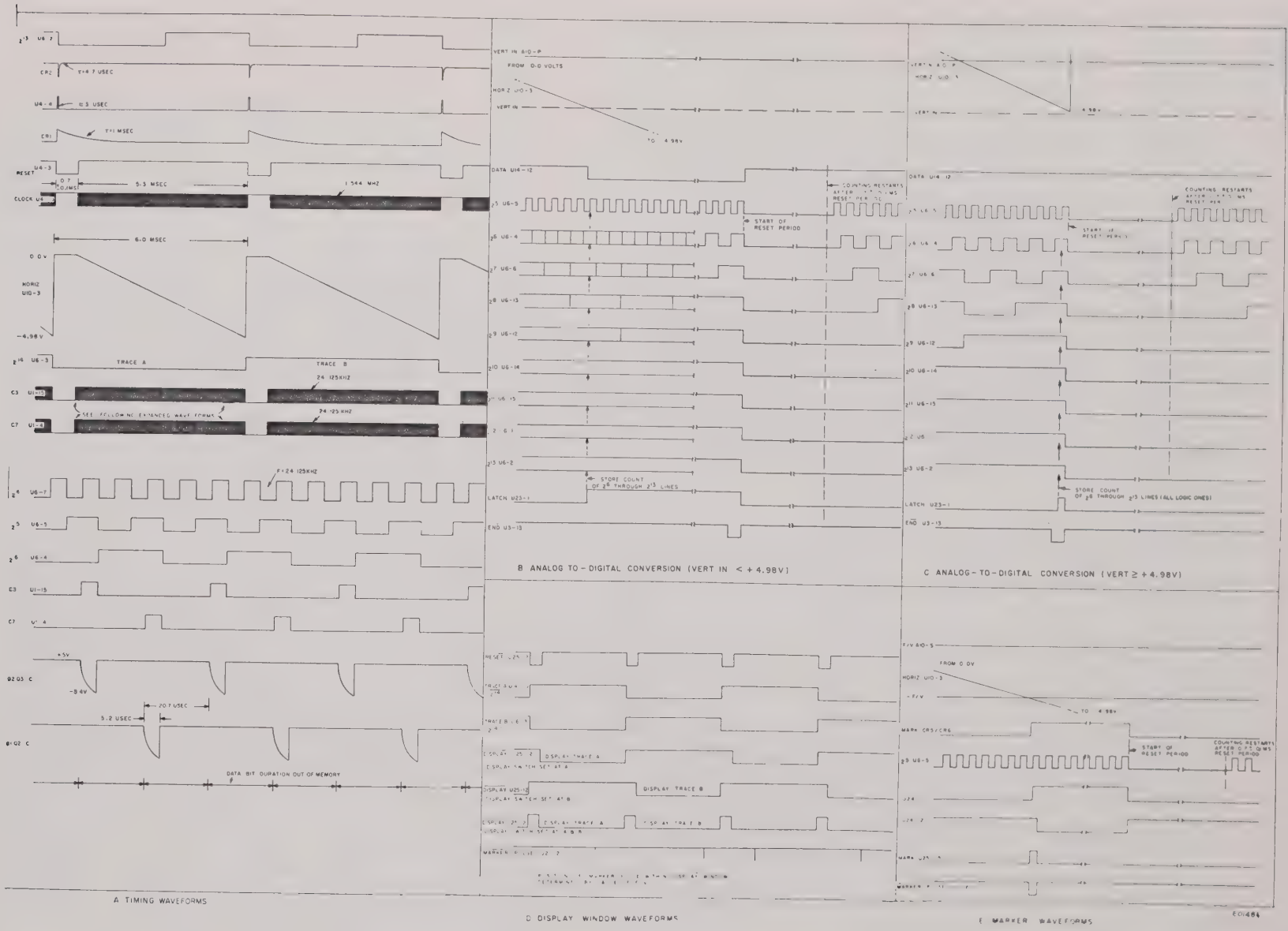


Figure 5–9. Digital Signal Processing Timing Diagram

SECTION 5

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Table 5—3. New And Old Data Control Signals

A AND/OR B DISPLAY	FUNCTION TEST SELECT	SIGNAL	NEW DATA	OLD DATA
ACTIVE	LEVEL, IMPEDANCE, or RL	MAN or SWEEP	**high** only for duration of "mark" during a trace period.	**low** only for duration of "mark" during a trace period.
ACTIVE	LEVEL, IMPEDANCE, or RL	ERL	**high** during entire trace period.	**low** during entire trace period.
ACTIVE	NOISE or NOISE/GND	_____	**high** during entire trace period.	**low** during entire trace period.
HOLD	_____	_____	**low** during entire trace period.	**high** during entire trace period.
CLEAR	_____	_____	**low** during entire trace period.	**low** during entire trace period.

5.116 **Intensity Control**

5.117 Transistors Q1 and Q4 comprise the intensity control circuit. A high $\overline{\text{DISPLAY}}$ cuts off transistor Q4 to break the current path on the INTEN line thereby blanking the display. A low $\overline{\text{MARKER PULSE}}$ supplies current to the MARKER line via transistor Q1 to intensify the trace during the $\overline{\text{MARKER PULSE}}$ time. Since the $\overline{\text{DISPLAY}}$ signal is independent of the NEW DATA and OLD DATA signals, a trace memory may be updated although not displayed.

5.118 **Vertical Deflection**

5.119 To appear on the display screen, the VERT IN signal must be:

a. detected by a comparator circuit,

b. strobed in and digitized by an input latch,

c. stored in a memory,

d. shifted out of the memory, and

e. reconverted into an analog signal to drive the vertical deflection amplifier.

5.120 Comparator U10B monitors the VERT IN signal together with the HORIZ ramp voltage. When the absolute value of HORIZ exceeds the VERT IN level a logic one is applied to the input latch circuit.

5.122 **Input Latch**

5.123 When the logic one is received by the input latch the value of the address word (formed by bits 2^6-2^{13}) equals the amplitude of HORIZ which, in turn, equals the amplitude of VERT IN. The next strobe (bit 2^5) pulse stores the logic one into flip-flop U23A. This action, in turn, stores the value of the address word into flip-flops U5A/B, U7A/B, U9A/B, and U11A/B. The input to flip-flop U23A is inhibited from changing by gate U22 until the next reset time. Thus, only one value can be stored in the input latch during each horizontal sweep. Figure 5—9B shows the timing waveforms for VERT IN less than the maximum value of HORIZ.

5.124 If the VERT IN signal is too large (an overrange indication), then the HORIZ ramp voltage never exceeds VERT IN. To ensure that the trace remains on the upper portion of the screen, the END pulse (bits 2^6-2^{13} all at logic one) occurs just prior to RESET period. The maximum count enters the input latch. Figure 5—9C shows the timing waveforms when VERT IN exceeds −5V.

5.125 The value stored in the input latch may be thought as the "most recent vertical data". During each horizontal sweep a "most recent vertical data" is presented to the recirculating memory.

5.126 **Recirculating Memory**

5.127 Whether the recirculating memory accepts the "most recent vertical data" depends on the NEW DATA and OLD DATA control signals received from the display logic. A high NEW DATA causes the memory to accept the "most recent vertical data" while a high OLD DATA instructs the memory to recirculate old data. Refer to Table 5−3 and note that the "most recent vertical data" will be accepted once during the selected trace time for level, impedance, and return loss measurements if the test signal is either manually tuned or swept. For other measurements, the "most recent vertical data" will be entered into each memory location. Thus, the display for a noise-type measurement appears as a straight line on the display screen. The absence of both NEW DATA and OLD DATA (A or B switch set at CLEAR) causes the value of zero to be entered in each memory location for that trace.

5.128 The recirculating memory consists of eight 512-bit shift registers contained within four integrated circuits U17,U18,U20, and U21 plus and-or gates U13A, B,C,D, and U15A,B,C,D. Timing for data shifting through the memory is provided by BCD-to-decimal decoder U1, inverters U2C and U2B, plus level translators Q2 and Q3. Figure 5−9A shows the pertinent memory timing waveforms.

5.129 Recall that the HORIZ ramp voltage requires one cycle of bits 2^6-2^{13}, or 256 time intervals. Therefore, for one horizontal sweep (bit $2^{14}=0$), the first 256 locations are assigned to trace A. On the alternate horizontal sweep (bit $2^{14}=1$) the second 256 locations are assigned to trace B. As the data words are continuously shifted through the memory they are applied to the vertical D/A converter for conversion into an analog signal.

5.130 **Vertical D/A Conversion**

5.131 D/A converter U12/U10D accepts the data word from the recirculating memory and develops a voltage proportional to the value of the data word. The VERT signal has a minimum amplitude of zero volts for a data word of 0 and a maximum amplitude of −4.98 V for a data word of 255. Thus the VERT signal level changes in multiples of 19.5-mV increments. These incremental changes are smoothed out by the feedback capacitor C25 before application to high voltage assembly A14.

5.132 RECEIVE SECTION, VIDEO PROCESSING DESCRIPTION

5.133 The video processing circuit receives the VERT and HORIZ signals from the digital signal processing circuit and amplifies these signals to drive the cathode ray tube (CRT). Two additional signals (INTEN and MARKER) are received to control the trace brightness. The video processing circuits generate all dc voltages to operate the CRT.

5.134 Figure 7−14 is a detailed schematic diagram of high voltage assembly A14 consisting of CRT power supply and deflection amplifier board A5 and high voltage board A16. These boards contain most of the video processing circuits. Figure 7−14 includes the interconnections between assembly A14 and the CRT.

5.135 **High Voltages**

5.136 The high voltages required for the CRT are generated using the ±15 volts from dc-dc converter PS3. The ±15 volts are first converted to 18.4-kHz ac voltages by Colpitts oscillator A5Q7 and complimentary amplifier A5Q8/Q9. Transistors A5Q12/Q13 ensure that the oscillator turns on slowly to prevent transients. Autotransformer A16T1 raises the 30 V p-p ac voltage to 2000 Vp-p. A secondary winding supplies 20 Vp-p (7.1 Vrms) as the filament voltage for the CRT.

5.137 The 2000 Vp-p is changed to a nominal −2kV by voltage doubler A16CR1CR2C1C2. The −2 kV is applied to voltage divider chain A16R2−R14 and A5R14 to supply the grid, cathode, and focus voltages.

5.138 Rectifier A5CR4 and capacitors C1,C2 function as an imperfect peak detector (due to a load current of about 2 mA). Thus the 374 Vp-p voltage changes into a dc level less than +200 V (approximately 175). The +200 V is used by the astigmatism control and the deflection amplifiers.

5.139 **Deflection Amplifier**

5.140 Transistors A5Q3/Q6 form a differential amplifier with a gain of 100 to amplify the HORIZ ramp voltage. Diodes A5CR1,CR2, resistors A5R15, R16, and capacitor A5C3 supply the bias voltage to constant current source A5Q5. The maximum output voltage is about 175 volts due to limits set by the +175 voltage (nominal +200 V). Horizontal gain potentiometer A5R21 selects how much of the HORIZ ramp voltage reaches the differential amplifier thus determining the actual gain. HORIZONTAL control A5R6 sets the trace horizontal position.

5.141 Transistors A5Q1/Q2, together with constant current source A5Q4, operate on the VERT signal in a similar manner as the horizontal deflection amplifier (described in paragraph 5.140). The outputs of the vertical differential amplifier are buffered by emitter followers A5Q10,Q11.

5.142 **Intensity**

5.143 The trace brightness is controlled by adjusting the potential difference between the cathode and grid 1 of the CRT. Part of the circuit is located on board A10 (intensity control shown on Figure 7−24) and the other part is located on board A16 (optical coupler shown on Figure 7−14). Figure 5−10 shows a simplified schematic of the intensity circuit for a clearer understanding of the circuit operation.

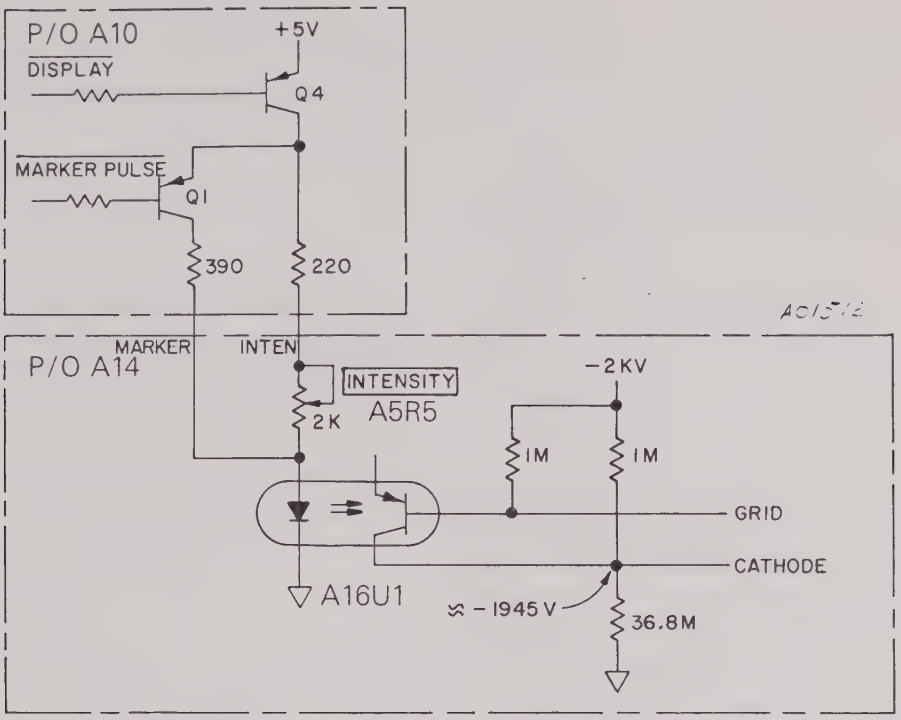


Figure 5—10. Intensity Circuit Simplified Schematic

5.144 With the $\overline{\text{DISPLAY}}$ signal at a logic one, transistor A10Q4 is cut off and no current flows through the diode of optical coupler A16U1. This results in maximum voltage difference between the cathode and grid 1 to blank out the CRT screen. A low $\overline{\text{DISPLAY}}$ allows a current set by INTENSITY control A5R5 to flow through the diode of the optical coupler. This reduces the potential difference between cathode and grid 1 and allows the trace to appear on the CRT screen. The larger the current, the brighter the trace becomes.

5.145 During the interval when $\overline{\text{MARKER PULSE}}$ goes to logic low, transistor A10Q1 injects additional current into the optical coupler diode. This results in additional brightness of the trace for the duration of the $\overline{\text{MARKER PULSE}}$.

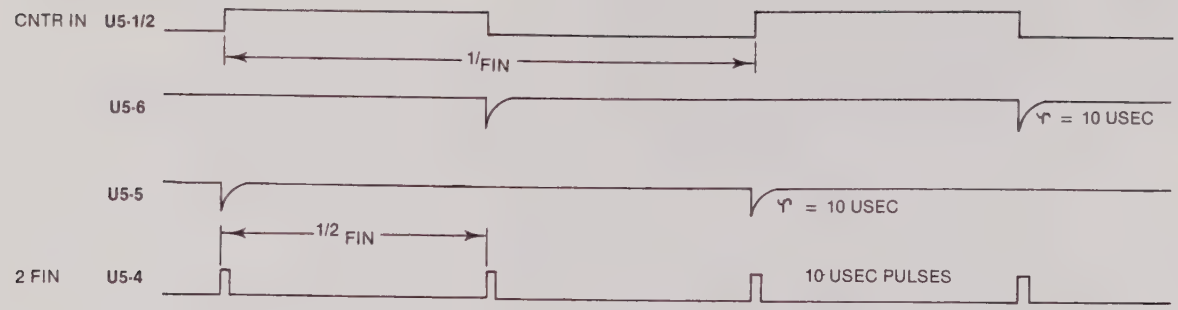
5.146 RECEIVE SECTION, FREQUENCY PROCESSING DESCRIPTION

5.147 The frequency processing circuits receive the CNTR IN signal from the transmit section and display the CNTR IN frequency on a four-digit, seven-segment display with an accuracy of ±1 Hz. The CNTR IN signal is a square wave version of either the transmit or the receive signal. Figure 7—16 is a detailed schematic diagram of the frequency counter and display board A6.

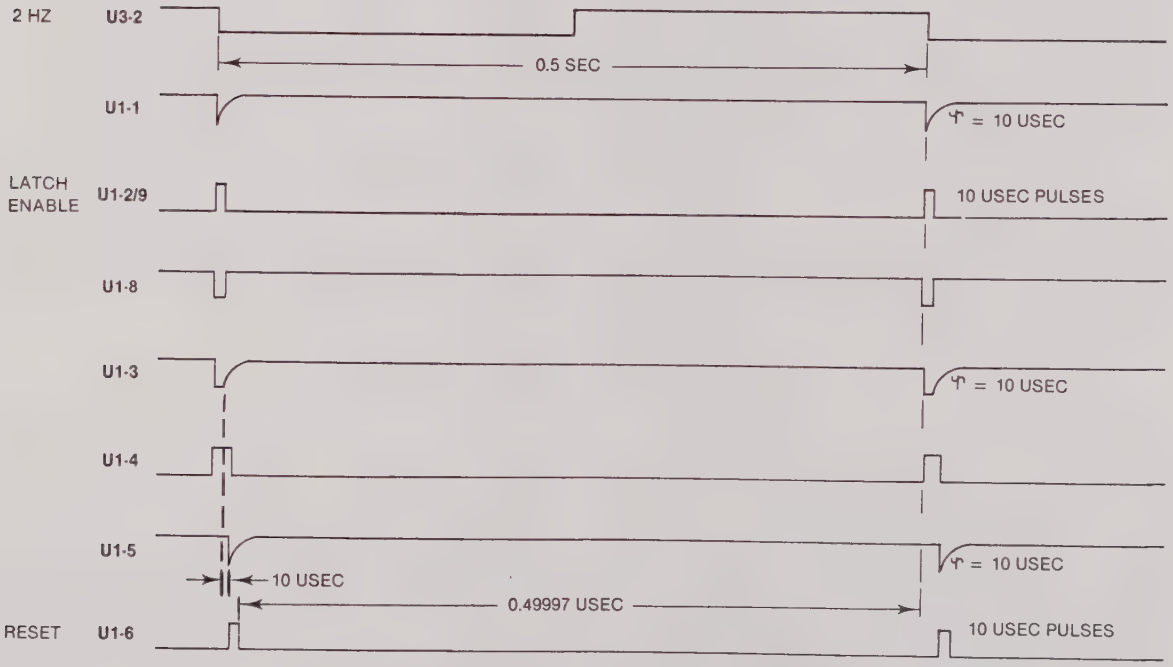
5.148 The CTR IN frequency is doubled and counted during a 0.5 second time base (2 Hz). Thus the accumulated count equals the input frequency. The time base is obtained from a 163.84-kHz crystal oscillator. The counter supplies the frequency count serially as a seven-segment code and four multiplexing outputs.

5.149 The "e" and "g" segment outputs are sensed by the leading zero suppression circuit for an e,g combination corresponding to a digit zero. The zero is suppressed if this digit and previous digits were all zeroes. The least significant digit is never suppressed. The multiplexing outputs strobe the display digits A (msd) through D (lsd) at a 1-kHz rate to present a flicker-free display.

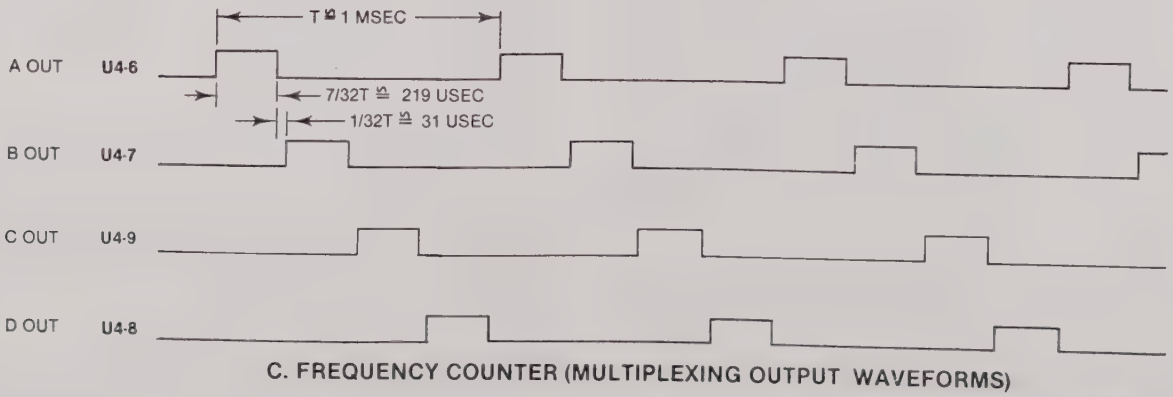
5.150 Figure 5—11 illustrates the timing waveforms for the frequency doubler, the frequency display timing and the multiplexing outputs. Note that the time axis is not proportionally scaled.



A. FREQUENCY DOUBLER



B. FREQUENCY DISPLAY TIMING



C. FREQUENCY COUNTER (MULTIPLEXING OUTPUT WAVEFORMS)

CO1513

Figure 5—11 Frequency Counter And Display Waveforms

5.151 **Frequency Doubler**

5.152 Diodes CR5 and CR6, together with gates U5A and U5B, double the CNTR IN frequency. Frequency doubling occurs by differentiating both edges of the square wave input and producing 10-microsecond pulses as shown in Figure 5−11A. The 2FIN pulse train is the clock input to frequency counter U4.

5.153 **Frequency Display Timing**

5.154 The time base is obtained from 163.84-kHz crystal oscillator Y1/U1F buffered by inverter U1E. Dividers U2 and U3 reduce the crystal frequency to 2-Hz. The 2-Hz signal is used as the counter time base. Diodes CR1, CR2, CR3 and inverters U1A-D provide the frequency counter with the proper latch and reset timing signals (see Figure 5−11B). The series of differentiators and delay produce a 10-microsecond LATCH ENABLE every 500 milliseconds and a 10 microsecond RESET trailing the ENABLE LATCH by 10 microseconds. The RESET also occurs every 500 milliseconds.

5.155 **Frequency Counter**

5.156 Frequency counter U4 consists of a 4-digit counter, an internal output latch, a BCD-to-7-segment decoder, and an internal multiplexer. The multiplexer has its own free-running oscillator. The multiplexing outputs select the digit to be displayed (whose value is then appearing on the seven-segment outputs).

5.157 **Leading Zero Suppression**

5.158 A digit zero may not be displayed if gates U5C and U7B sense the presence of a high e segment and a low g segment. Gate U5D and inverter U7D prevent displaying a zero for the most significant digit. Gates U6A, U6D and inverter U7E, together with flip-flop U8B, inhibit the display of a zero for digit B if digit A is also zero. Similarly gates U6B, U6C and inverter U7F, in conjunction with flip-flop U8A, do not allow a zero for digit C if both digits A and B are zeroes.

5.159 Digit drivers Q1-Q4 provide the ground signal to select the display digit. The selected display digit shows the value present on the seven-segment outputs. Digit driver Q4 is controlled directly by the D OUT signal, therefore the least significant digit is never suppressed.

5.160 **POWER SECTION, DETAILED DESCRIPTION**

5.161 The power section generates and distributes dc voltages required for operation of the Level Tracer. Sheet 1 of Figure 7−26 shows the power distribution and sheet 2 of the same figure contains the detailed schematic diagrams of power supply PS1 and voltage regulator A11U1.

5.162 The power section consists of the following items.

a. Power supply PS1, generates the +6.8 V applied to batteries BT1, BT2 and to dc-dc converters A11PS2 and PS3. (Dc-dc converter PS3 is mounted directly on the chassis).

b. Batteries BT1 and BT2 supply the +6.8 V when the Level Tracer is operating while **not** connected to an ac power source. If the Level Tracer is connected to ac power, then the batteries are being charged continuously whether or not the Level Tracer is turned on.

c. Dc-dc converters A11PS2 and PS3 supply +15 volts. Converter PS3 ±15 V outputs are used only by the CRT power and deflection board A5. The ±15 V outputs from dc-dc converter A11PS2 are used by the rest of the circuits in the Level Tracer. The dc-dc converters are sealed units and are non-repairable.

d. Voltage regulator A11U1 uses +15 V and +6.8 V to provide +5 V for the logic circuits contained in the Level Tracer.

e. A meter circuit on board A4 monitors the difference between the +6.8 V from the batteries and the +5 V from the regulator. Then the meter displays the capacity of the batteries. The meter needle moves to the left toward the red zone as the battery voltage falls below +6.8 V.

5.163 POWER SUPPLY PS1

5.164 Sheet 2 of Figure 7−26 shows that the power supply circuit consists of an integrated circuit voltage regulator configured as a series-pass regulator. The regulator may be thought of as a non-inverting operational amplifier with a fixed reference input voltage. The reference voltage is obtained from the internal voltage of U1 and is divided down by resistors R8 and R12. The output voltage may be adjusted via feedback resistor R11.

5.165 VOLTAGE REGULATOR A11U1

5.166 Voltage regulator A11U1 is also an integrated circuit voltage regulator configured as a series-pass regulator. It may be looked upon as a voltage follower operational amplifier. The output voltage is controlled by changing the reference input voltage via resistor R6. This type of adjustment is necessary since a voltage follower has no voltage gain. The output voltage is normally set at +5 V.

SECTION 6

MAINTENANCE

6.1 This section contains information needed to calibrate and maintain the Model 8100 Level Tracer. Battery replacement instructions are also included.

6.2 BATTERY REPLACEMENT

6.3 The batteries in the Level Tracer can be charged and discharged several hundred times before replacement is required. If the Level Tracer will not operate on battery power, check the front panel fuse. Should the fuse be defective then replace the fuse and recharge the batteries. If the fuse is okay, replace the batteries as follows.

1. Remove the Level Tracer case cover.

2. Ensure that POWER switch is at OFF.

3. Loosen and remove the four screws (one at each corner) securing the Level Tracer to the carrying case.

CAUTION

Do not place the Level Tracer on its end when out of the carrying case. The neck of the CRT could be damaged.

4. Carefully lift out the Level Tracer and place it on a work surface.

5. Loosely secure the screws in the carrying case for safekeeping.

6. Disconnect the four wires from the batteries.

7. Loosen and remove the four sets of screws and washers holding the battery bracket to the chassis.

8. Lift up the battery bracket and remove the batteries.

9. Place new batteries inside battery bracket. Refer to illustration on battery bracket for battery orientation.

10. Attach the battery bracket with four sets of 6-32 screws together with flat and split washers.

11. Connect the purple leads to the battery positive terminals and the green leads to the negative terminals as shown on the bracket illustration.

12. Connect a digital voltmeter to E6 (positive lead) and E8 (ground lead) on board A11.

13. Set Level Tracer POWER switch at ON.

14. Observe that digital voltmeter indicates between +5.5V and +6.8V.

15. Set POWER switch at OFF.

16. Disconnect digital voltmeter.

17. Replace Level Tracer in its carrying case.

6.4 LEVEL TRACER CALIBRATION

6.5 The following paragraphs provide a complete set of adjustment procedures for the Level Tracer. These procedures can be used for periodic maintenance or after repair of the unit. These procedures require precision laboratory test equipment. Personnel performing these procedures must be familiar with the type of test equipment recommended. No attempt to calibrate the Level Tracer should be made without the proper test equipment or qualified personnel.

6.6 The Level Tracer calibration is presented as a series of check and adjustment procedures for easy reference. The entire series of procedures must be performed in the order presented since most of the procedures depend upon the adjustments made in previous procedures. In addition, the procedures assume that positions of the switches and controls remain in their previously specified positions unless specifically instructed to set at new positions.

6.7 TEST EQUIPMENT REQUIRED

6.8 Table 6—1 list the type of equipment required to calibrate the Level Tracer. Select test equipment that meets the requirements listed in Table 6—1. Common tools and cables are not listed.

6.9 PREPARATION FOR CALIBRATION

6.10 Preparation for calibration consists of removing the Level Tracer from its carrying case to expose all adjustments. Parts location diagrams (Figure 7—12, 7—13, 7—19, and 7—21) show the adjustment locations. Before beginning calibration of the Level Tracer all test equipment should be allowed to warm-up for the period specified by the test equipment manufacturers. For access to adjustments, perform the following steps.

1. Remove the Level Tracer case cover.

2. Loosen and remove the four screws (one at each corner) securing the Level Tracer to the carrying case.

CAUTION

Do not place the Level Tracer on its end when out of the carrying case. The neck of the CRT could be damaged.

3. Carefully lift out the Level Tracer and place it on a work surface.

4. Loosely secure the screws in the carrying case for safekeeping.

5. Loosen and remove two sets of screws and washers securing the pc card retainer (on right-hand side of Level Tracer).

6. Remove the pc card retainer.

7. Loosely secure the screws in the pc card retainer.

6.11 POWER SUPPLY CALIBRATION

1. Connect the power cable to the Level Tracer and a power source.

2. Set the POWER switch at ON. Allow the Level Tracer to warm-up for half an hour.

3. Place the Level Tracer face down on two blocks to avoid bending the power cord.

4. Connect the digital voltmeter to E6 (positive lead) and E8 (ground) on board A11.

5. Observe that the digital voltmeter indicates +6.70 ±0.05 V. If necessary, adjust V ADJ potentiometer R11 on power supply PS1 to obtain +6.70±0.05 V. V ADJ potentiometer R11 is accessible through a hole in board A11.

NOTE

If the dc level is less than +5.5 V then one or both batteries may need to be replaced. Refer to paragraph 6.2.

6. Connect the digital voltmeter to E4 (+5V) and E2 (GND) on board A11.

7. Observe that the digital voltmeter indicates +5.0 ±0.1 V. If necessary, adjust +5 V ADJ potentiometer R6 on board A11 to obtain +5.0±0.1 V.

8. Disconnect the digital voltmeter.

9. Set the Level Tracer upright.

10. Proceed to the transmit section calibration (paragraph 6.12).

Table 6—1. Test Equipment Required

EQUIPMENT	USE
Digital Voltmeter	To monitor dc voltages of 10 volts with an accuracy of ±10 millivolts.
Analog Voltmeter	To monitor ac voltages (+10 dBm to −40 dBm into 600 ohms) with an accuracy of ±0.1 dB.
Distortion Analyzer	To measure distortion of 2% with an accuracy of ±3% or better.
Audio Oscillator	To supply reference levels (+10 dBm to −40 dBm into 600 ohms) with an accuracy of ±0.1 dB. Must have an output impedance of 600-ohms.
Oscilloscope	To monitor waveforms for symmetry and duty cycle. Use an oscilloscope with a bandwidth of at least 5MHz.
8100 Extender Test Board Northeast Electronics Part Number C8100-00-021	To make test points on pc boards easily accessible.
Precision resistor 600-ohms, 0.05%	To provide accurate termination.

6.12 TRANSMIT SECTION CALIBRATION

1. Set the Power switch at OFF.

2. Remove transmitter board A9 from the card cage.

3. Ensure that all switches on the extender test board are on.

4. Insert the extender test board into connector XA9 and mount transmitter board A9 on the extender test board.

5. Set the POWER switch at ON.

6. Connect the digital voltmeter to TP1 (positive lead) and to TP11 (ground lead) on transmitter board A9.

7. Set the Level Tracer controls as follows:

a. DISPLAY FREQUENCY at SEND,

b. SIGNAL at MAN,

c. FUNCTION test select at LEVEL,

d. SF SUPP at OFF,

e. IMPEDANCE at 600 OHMS, and

f. SWEEP SPEED at SLOW.

8. Set 200 Hz potentiometer R12 on transmitter board A9 fully counterclockwise.

9. Adjust the FREQ TUNING control fully counterclockwise.

10. Observe that the FREQUENCY-Hz display reads 185 ± 3 Hz. If necessary, adjust FREQ potentiometer R14 on transmitter board A9 to obtain 185 ± 3 Hz.

11. Disconnect the digital voltmeter and adjust the FREQ TUNING control to obatin 200 ± 1 Hz on the FREQUENCY-Hz display.

12. Connect the oscilloscope to TP2 (positive lead) and to TP11 (ground lead) on transmitter board A9.

13. Observe that the oscilloscope shows a 200 Hz square wave with 50% duty cycle. If necessary, adjust RATIO potentiometer R13 to obtain a 50% duty cycle square wave as seen on the oscilloscope.

14. Disconnect the oscilloscope.

15. Connect a precision 600-ohm resistor across the TRANSMIT section LINE 1 TIP and RING jacks.

16. Connect the distortion analyzer to the TRANSMIT section LINE 1 TIP and RING jacks. Also connect the distortion analyzer ground terminal to the Level Tracer GROUND terminal.

17. Set the Level Tracer transmit level at +10 dBm (LEVEL dBm switch settings of 10 and 0).

18. Adjust the FREQ TUNING control to obtain 2000 ± 5 Hz on the FREQUENCY-Hz display.

19. Use the distortion analyzer to measure less than 2% distortion on the Level Tracer output. If necessary, alternately adjust RATIO potentiometer R13 and DIST potentiometer R16 on transmitter board A9 to obtain less than 2% distortion.

20. Tune the Level Tracer to 200 ± 10 Hz and to 4000 ± Hz. Measure less than 2% distortion at these frequencies. If necessary, retune the Level Tracer to 2000 ± 5 Hz and repeat step 19.

21. Disconnect the distortion analyzer; do not remove the precision resistor.

22. Connect the analog voltmeter to the TRANSMIT section LINE 1 TIP and RING jacks.

23. Set the Level Tracer transmit level at 0 dBm (LEVEL dBm switch settings of 0 and 0).

24. Adjust the FREQ TUNING control to obtain 1004 ± 1 Hz on the FREQUENCY-Hz voltmeter display.

25. Observe that the analog voltmeter indicates 0.00 ± 0.05 dBm. If necessary, adjust LEVEL potentiometer R77 on transmitter board A9 to obtain reading of 0.00 ± 0.05 dBm.

26. Disconnect the analog voltmeter and remove the precision resistor.

27. Connect the digital voltmeter to pin N (positive lead) and pin B (ground lead) on the extender test board.

28. Adjust the FREQ TUNING controls to obtain 4100 ± 10 Hz on the FREQUENCY-Hz display.

29. Observe that the digital voltmeter indicates 4.90 ± 0.01 V. If necessary, adjust F/V potentiometer R63 on transmitter board A9 to obtain 4.90 ± 0.01 V.

30. Disconnect the digital voltmeter.

31. Set the POWER switch at OFF.

32. Remove the extender test board and replace transmitter board A9 into connector XA9.

33. Proceed with the receive section calibration (paragraph 6.13).

6.13 RECEIVE SECTION CALIBRATION

1. Remove receiver board A8 from the card cage.

2. Ensure that all switches on the extender test board are on.

3. Insert the extender test board into connector XA8 and mount receiver board A8 on the extender test board.

4. Set the Level Tracer INPUT switch at LINE 1 BRIDGE and dB SCALE switch at X1.

5. Set the POWER switch at ON.

6. Adjust the FREQ TUNING control to obtain 1004 ±1 Hz on the FREQUENCY-Hz display.

7. Set up the CMRR test connections shown in Figure 6−1. Use a precision 600-ohm resistor.

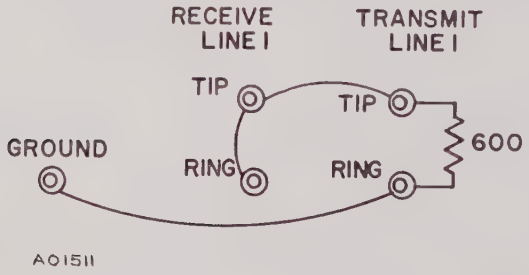


Figure 6−1. CMRR Test Connections

8. Connect the analog voltmeter to TP1 (positive lead) and TP4 (ground lead) on receiver board A8.

9. Set the Level Tracer transmit level at +10 dBm (LEVEL dBm switch settings of 10 and 0).

10. Observe that the analog voltmeter reads less than 1.5 millivolt. If necessary, adjust CMRR potentiometer R5 on receiver board A8 to obtain a reading of less than 1.5 millivolt.

11. Disconnect the analog voltmeter and the CMRR test connections of Figure 6−1.

12. Connect the audio oscillator to the RECEIVE section LINE 1 TIP and RING jacks.

13. Connect the analog voltmeter to the RECEIVE section LINE 1 TIP and RING jacks.

14. Set INPUT switch at LINE 1 TERM and DISPLAY FREQUENCY switch at REC.

15. Connect digital voltmeter to TP3 on receiver board A8. Use TP4 as ground reference.

16. Adjust audio oscillator frequency to 1004±1 Hz as indicated on the Level Tracer FREQUENCY-Hz display.

17. Adjust the audio oscillator output level to +8.0 dB as indicated on the analog voltmeter. Record the dc level reading obtained on the digital voltmeter. (Reading should be approximately −8 V).

18. Readjust the audio oscillator output level to −12.0 dB as indicated on the analog voltmeter. Record the dc level reading obtained on the digital voltmeter. (Reading should be approximately −800 mV).

19. Again readjust the audio oscillator output level to −32.0 dB as indicated on the analog voltmeter. Record the dc level reading obtained on the digital voltmeter. (Reading should be approximately −80 mV.)

20. Observe that the recorded reading in step 17 is 10 times as large as the recorded reading of step 18. Similarly observe that the recorded reading in step 18 is 10 times as large as the recorded reading of step 19. If necessary, adjust OFFSET potentiometer R50 on receiver board A8 to obtain a 10.0±0.2 to 1 change in the dc level as the audio oscillator output level changes by 20 dB.

21. Repeat steps 17 through 20 until no further improvement is obtained with additonal offset adjustments.

22. Connect the digital voltmeter to pin 18 (positive lead) and pin 2 (ground lead) on the extender test board.

23. Adjust the audio oscillator output level to 0.0 dB as indicated on the analog voltmeter.

24. Observe that the digital voltmeter indicates 0±5 mV. If necessary, adjust DB GAIN potentiometer R58 on receiver board A8 to obtain 0±5 mV.

25. Disconnect the digital voltmeter. Do not disconnect the audio oscillator or the analog voltmeter.

26. Proceed with the display section calibration (paragraph 6.14).

6.14 DISPLAY SECTION CALIBRATION

WARNING

The CRT power supply and deflection amplifier board A5 contains high voltages up to +2000 volts. Do NOT remove the plexiglass shield, use only insulated alignment tools.

1. Set the DISPLAY switch at A.

2. Set the memory trace A switch at CLEAR then at ACTIVE.

3. Set the SIGNAL switch at SWEEP and the DISPLAY FREQUENCY switch at SEND.

4. Adjust the VERTICAL control to position the trace somewhere near the 0 dB reference line.

5. Adjust the HORIZONTAL control to center the trace.

6. Adjust the FOCUS and the INTENSITY controls to obtain a sharp trace.

7. Set the SIGNAL switch at MAN and the memory trace A switch at HOLD.

8. Adjust the FREQ TUNING control to obtain 1500 ±250 Hz on the FREQUENCY Hz display.

9. Adjust the INTENSITY control so that the frequency marker stands out clearly.

10. Observe that the frequency marker has a round shape. If necessary, adjust ASTIG potentiometer R23 on board A5 to obtain a round frequency marker. Readjust the FOCUS and INTENSITY controls as required.

11. Set the SIGNAL switch at SWEEP and the memory trace A switch at ACTIVE.

12. Observe that the analog voltmeter still indicates 0.0 dB. If necessary, readjust the audio oscillator output level.

13. Toggle dB SCALE switch back and forth between X¼ and X1 and observe that the trace shows no change in level. If necessary, **fine** adjust DB GAIN potentiometer R58 on receiver board A8 so that no change in level is observed on the trace as the dB SCALE switch is toggled between X¼ and X1.

14. Set dB SCALE switch at X1.

15. Set the DISPLAY switch at A&B and the memory trace B switch at CLEAR.

16. Adjust the audio oscillator output level to +4.0 dB as indicated on the analog voltmeter.

17. Allow trace A to be completely updated then set the memory trace A switch at HOLD.

18. Set the memory trace B switch at ACTIVE.

19. Adjust the audio oscillator output level to −28.0 dB as indicated on the analog voltmeter.

20. Allow trace B to be completely updated, then set the memory trace B switch at HOLD.

21. Observe that the two traces appear on the display screen. If necessary, adjust the VERTICAL control to position the two traces on the screen.

22. Observe a separation of 32.0±0.5 dB between the two traces. If necessary, adjust VERT potentiometer R19 on board A5 to obtain a 32.0±0.5 dB separation.

23. Set the memory trace A at ACTIVE and the memory trace B at CLEAR.

24. Adjust the audio oscillator output level to 0.0 dBm as indicated on the analog voltmeter.

25. Adjust the VERTICAL control to position trace B on the "clear" graticule line (line below the −32 dB graticule).

26. Observe that trace A is on the 0 dB reference graticule line. If necessary, adjust 0 REF potentiometer R74 on receiver board A8 to position trace A on the 0 dB reference graticule line.

27. Set the SIGNAL switch at MAN.

28. Adjust the FREQ TUNING control to obtain 200 ±1 Hz on the FREQUENCY-Hz display.

29. Set the memory trace B switch at CLEAR.

30. Adjust HORIZONTAL control to make left-hand side of trace visible.

31. Set the memory trace A switch at CLEAR then toggle the memory trace A switch to ACTIVE then back to HOLD.

32. Observe that a pulse is present on the left-hand side of the trace. This is the 200-Hz reference mark. If no pulse is present, repeat step 31.

33. Set the memory trace B switch at ACTIVE.

34. Set the SIGNAL switch at SWEEP.

NOTE

Step 35 may need to be repeated several times to obtain the correct result. Between adjustments, toggle memory trace B switch to CLEAR then back to ACTIVE.

35. Observe that the left-hand side of the sweep extends slightly past the 200-Hz reference mark. If necessary, adjust 200 Hz potentiometer R12 transmitter board A9 to obtain a trace that sweeps just slightly past the 200-Hz reference mark.

36. Set memory trace B switch at CLEAR.

37. Set the SIGNAL switch at MAN.

38. Adjust the FREQ TUNING control to obtain 1000 ± 1 Hz on the FREQUENCY-Hz display.

39. Toggle the memory trace A switch to CLEAR then back to ACTIVE.

40. Slowly adjust the FREQ TUNING control to obtain 3000 ± 1 Hz on the FREQUENCY-Hz display. Do not exceed 3000 ± 1 Hz; if you do, repeat steps 38 through 40.

41. Set the memory trace A switch at HOLD.

42. Adjust the FREQ TUNING control to obtain 2000 ± 1 Hz on the FREQUENCY-Hz display.

43. Adjust the HORIZONTAL control to position the left-hand side of trace A on the 1.0 kHz vertical graticule.

44. Observe that the right-hand side of trace A lies on the 3.0 kHz vertical graticule. If necessary, adjust HORIZ potentiometer R21 on board A5 to position the right-hand side of trace A on the 3.0 kHz vertical graticule. Readjust the HORIZONTAL control as required to maintain the left-hand side of trace A on the 1.0 KHZ vertical graticule line. When the horizontal gain is properly adjusted, the frequency marker lies on the 2.0 KHZ vertical graticule line.

45. Disconnect the audio oscillator and the analog voltmeter.

46. Patch the TRANSMIT section LINE 1 TIP and RING jacks to the RECEIVE section LINE 1 jacks (tip to tip and ring to ring).

47. Set the transmit level at 0 dBm (LEVEL dBm switch settings of 0 and 0).

48. Set the SIGNAL switch at SWEEP and the memory trace A switch at ACTIVE.

49. Observe that trace A indicates 0.0 ± 0.5 dB.

50. Check several other transmit level settings and observe that trace A tracks the transmit level with an accuracy of ±0.5 dB.

51. If incorrect results were obtained in steps 49 and/or 50, repeat all the calibration procdures, Otherwise, proceed to ERL noise signal calibration (paragraph 6.15).

6.15 ERL NOISE SIGNAL CALIBRATION

1. Short circuit the RECEIVE section LINE 1 TIP and RING jacks together.

2. Set FUNCTION test select switch at RL and FUNCTION range select switch at 0 (RL).

3. Allow trace A to be completely updated, then set the memory trace A switch at HOLD.

4. Set memory trace B switch at ACTIVE.

5. Set SIGNAL switch at ERL.

6. Allow trace B to stabilize.

7. Observe that trace B hovers about trace A. If necessary, adjust ERL potentiometer R62 on transmitter board A9 to position trace B over trace A. Excursions of trace B should be symmetrical about trace A.

8. Remove short circuit from the RECEIVE section LINE 1 TIP and RING jacks.

9. Set SIGNAL switch at SWEEP.

10. Proceed with the IMPEDANCE calibration (paragraph 6.16).

6.16 IMPEDANCE CALIBRATION

1. Connect a precision 600-ohm resistor across the LINE 1 TIP and RING jacks of the RECEIVE section.

2. Set the FUNCTION test select switch at IMPEDANCE and the FUNCTION range select switch at X1.

3. Allow trace B to be completely updated.

4. Observe that trace B indicates 600 ± 10 ohms. If necessary, adjust OHMS potentiometer R64 on receiver board A8 to obtain 600 ± 10 ohms.

5. Short circuit RECEIVE section LINE 1 TIP and RING jacks together.

6. Observe that trace B indicates 0 ± 10 ohms. If necessary, remove short circuit and repeat step 4.

7. Remove short circuit and precision resistor.

8. Set POWER switch at OFF.

9. Remove the extender test board and replace receiver board A8 into connector XA8.

10. This completes the Level Tracer calibration. Replace the card retainer on the card cage and return the Level Tracer in its carrying case.

SECTION 7

DIAGRAMS

7.1 This section contains functional diagrams, parts location diagrams, and schematic diagrams for the Model 8100 Level Tracer.

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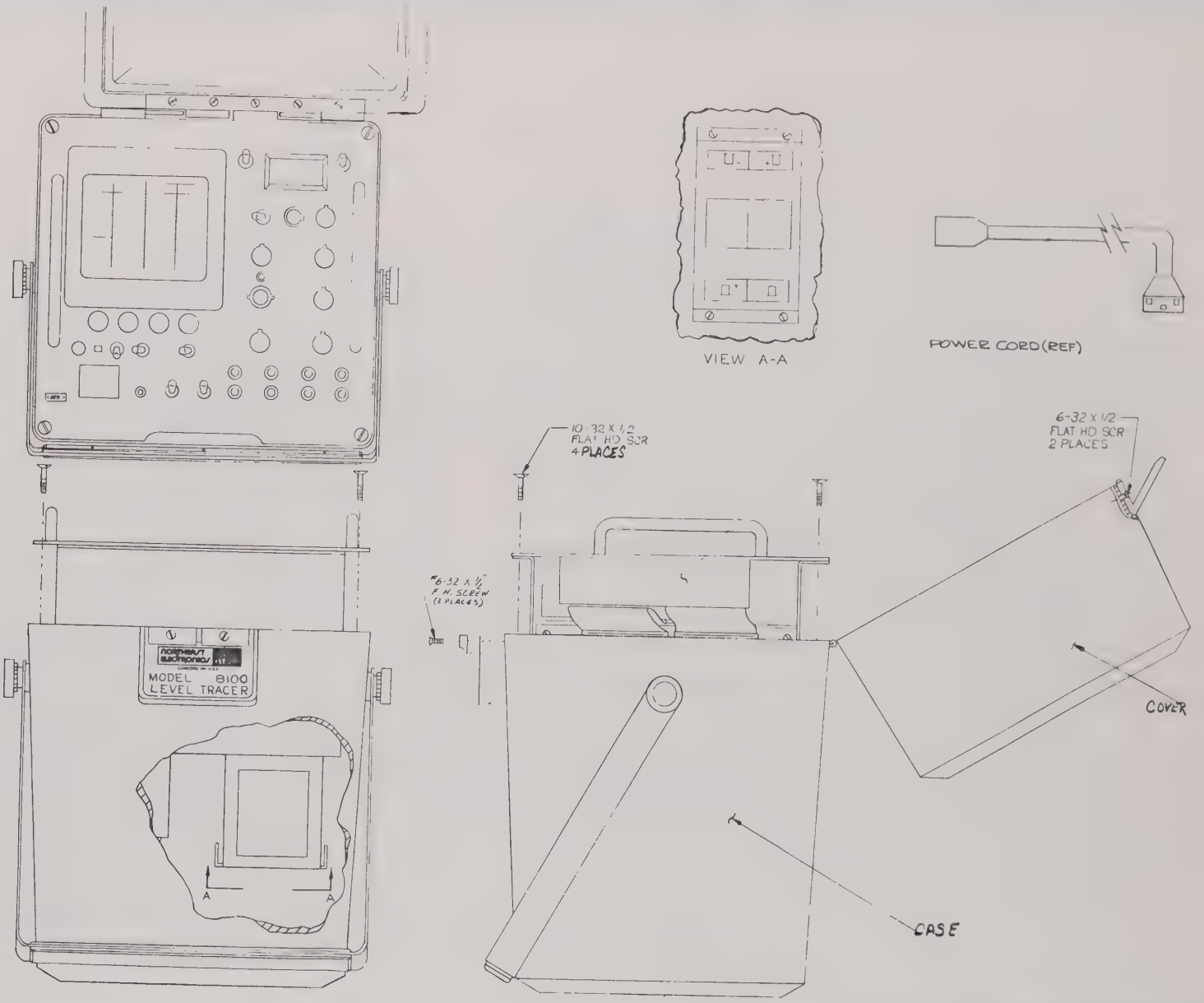
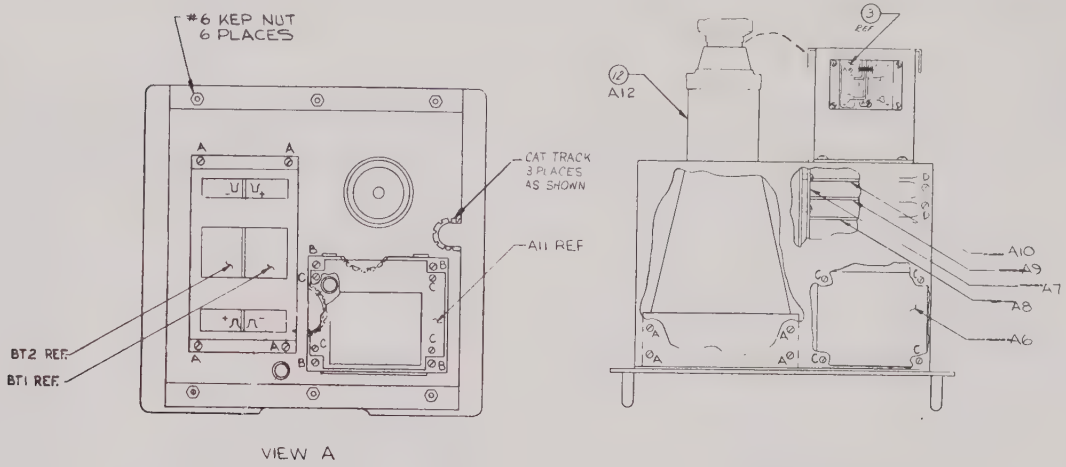
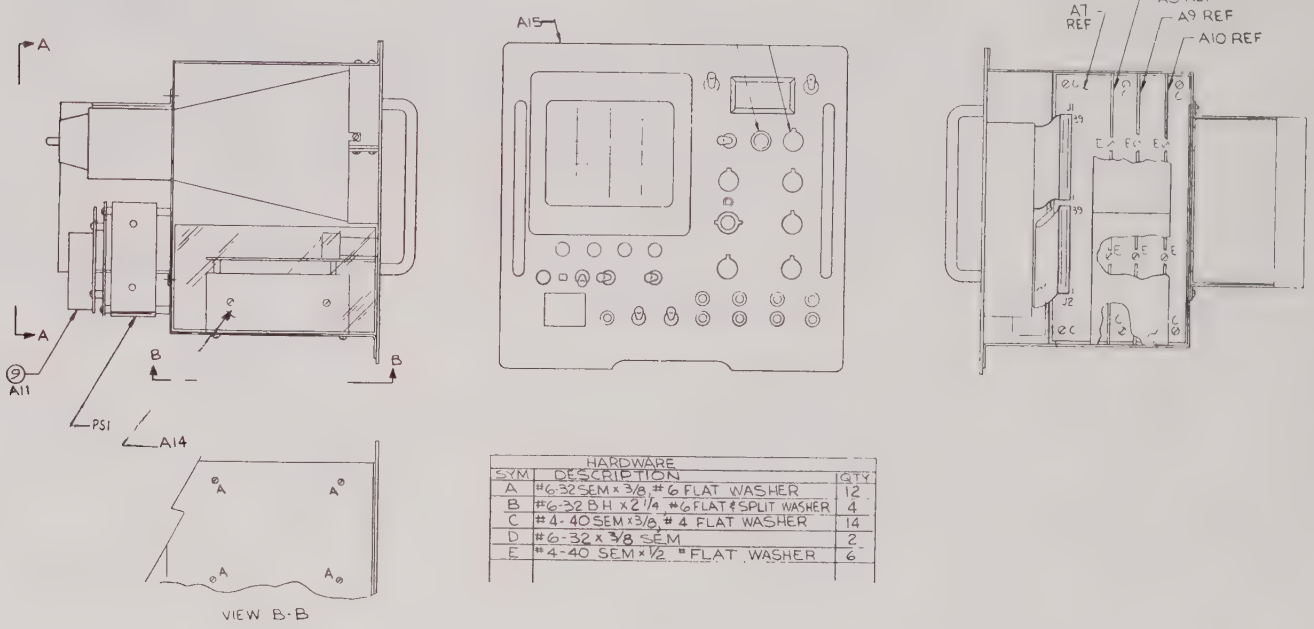


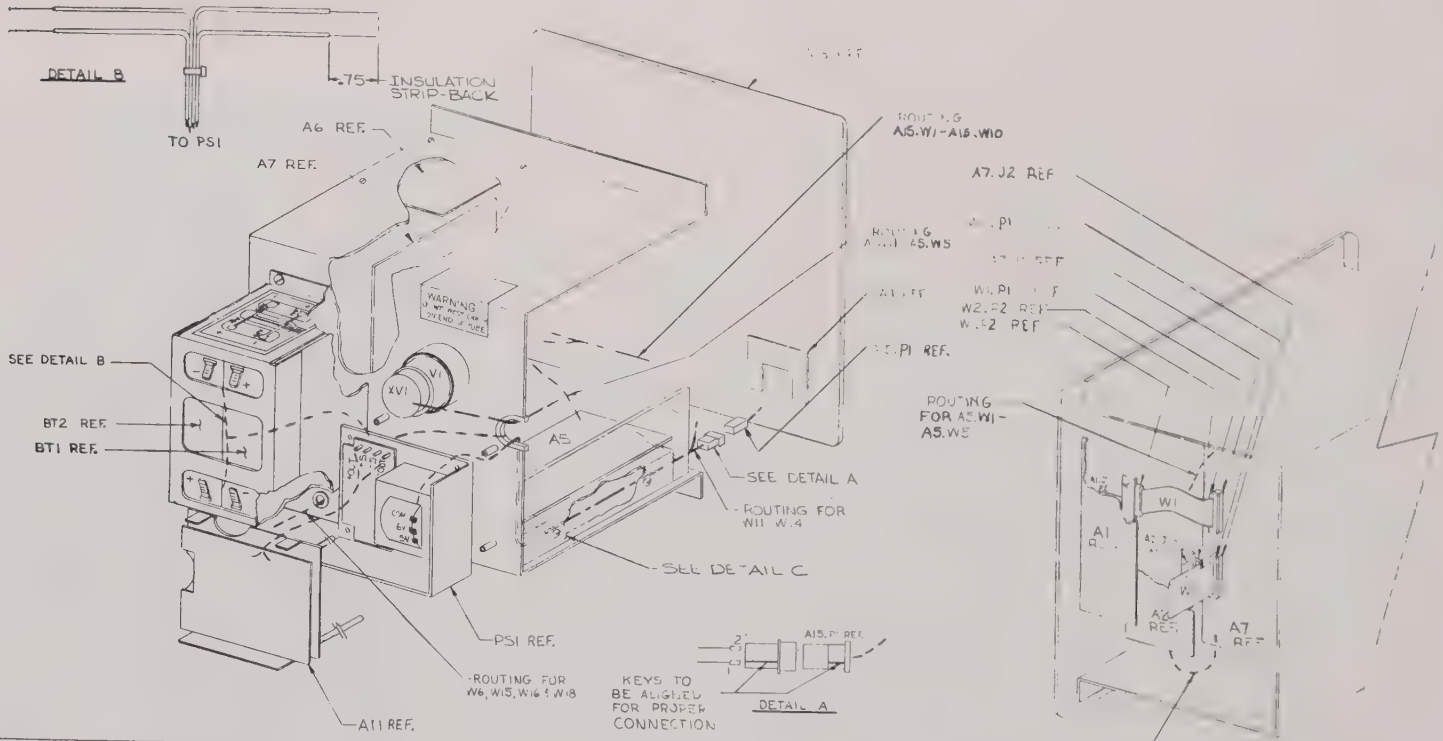
Figure 7—1. Level Tracer Overall Assembly





HARDWARE		
SYM	DESCRIPTION	QTY
A	#6-32 SEM x 3/8, #6 FLAT WASHER	12
B	#6-32 BH x 2 1/4 #6 FLAT & SPLIT WASHER	4
C	#4-40 SEM x 3/8, #4 FLAT WASHER	14
D	#6-32 x 3/8 SEM	2
E	#4-40 SEM x 1/2 " FLAT WASHER	6

Figure 7—2. Level Tracer Assembly (Sheet 1)

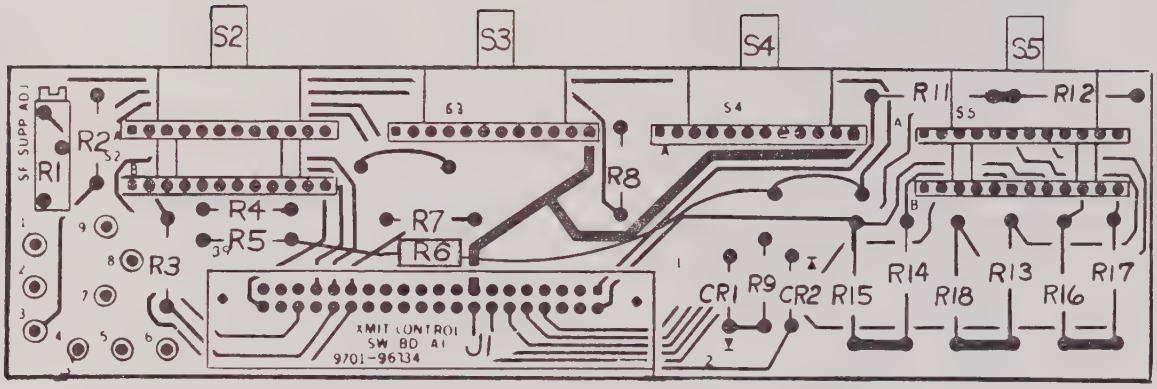


WIRE LIST (001)

WIRE NO.	COLOR	GA	APPROX LENGTH	SIGNAL NAME	FROM	NOTES	TO	NOTES
W1					XV1		V1	SEE NOTE 1
					P1	CABLE #1	A7.J1	
					P2		A11.J1	SEE NOTE 2
W2					P1	CABLE #2	A7.J2	
					P2		A2.J1	
W3	GRN	18STR	10"	GND	BT2.(-)		PSI(com)	SEE DETAIL B
W4	GRN	18STR	10"	GND	BT1.(-)		PSI(com)	
W5	GRN	20STR	4"	GND	PSI(com)		A11.8	FEM.Q.D.
W6	GRN	20STR	8"	GND	A11.2	FEM.Q.D.	A7.19	FEM.Q.D.
W7	GRN	20STR	15"	GND	A11.2		A5.18	FEM.Q.D.
W8	PRP	18STR	10"	BAT	BT2.(+)		PSI(com)	SEE DETAIL B
W9	PRP	18STR	10"	BAT	BT1.(+)		PSI(com)	
W10	PRP	20STR	4"	BAT	PSI(com)		A11.6	FEM.Q.D.
W11	SLT	22STR	18"	PWR (A)	A11.7	FEM.Q.D.	A4.1	FEM.Q.D.
W12	BRN	22STR	18"	PWR (B)	A11.5	FEM.Q.D.	A4.5	FEM.Q.D.
W13	WHT	20STR	18"	110 VAC (N)	PSI.(COM)	TWISTED PAIR	J1.2	SEE DETAIL A
W14	BLK	20STR	18"	110 VAC (LF)	PSI.(6V)		J1.1	
W15	RED	20STR	8"	+ 3V	A11.4	FEM.Q.D.	A7.22	FEM.Q.D.
W16	BLU	20STR	8"	+ 15 V	A11.1	FEM.Q.D.	A7.20	FEM.Q.D.
W17	BLU	20STR	15"	+ 15 V	A11.1		A5.16	FEM.Q.D.
W18	ORN	20STR	8"	- 15 V	A11.3	FEM.Q.D.	A7.21	FEM.Q.D.
W19	ORN	20STR	15"	- 15V	A11.3		A5.17	FEM.Q.D.
W20	GRN	20STR	4"	GND	A7.4	FEM.Q.D.	A6.2	FEM.Q.D.
W21	RED	20STR	4"	+ 5V	A7.1	FEM.Q.D.	A6.3	FEM.Q.D.
W22	WHT/SLT	22STR	4"	CNTR IN	A7.2	FEM.Q.D.	A6.1	FEM.Q.D.

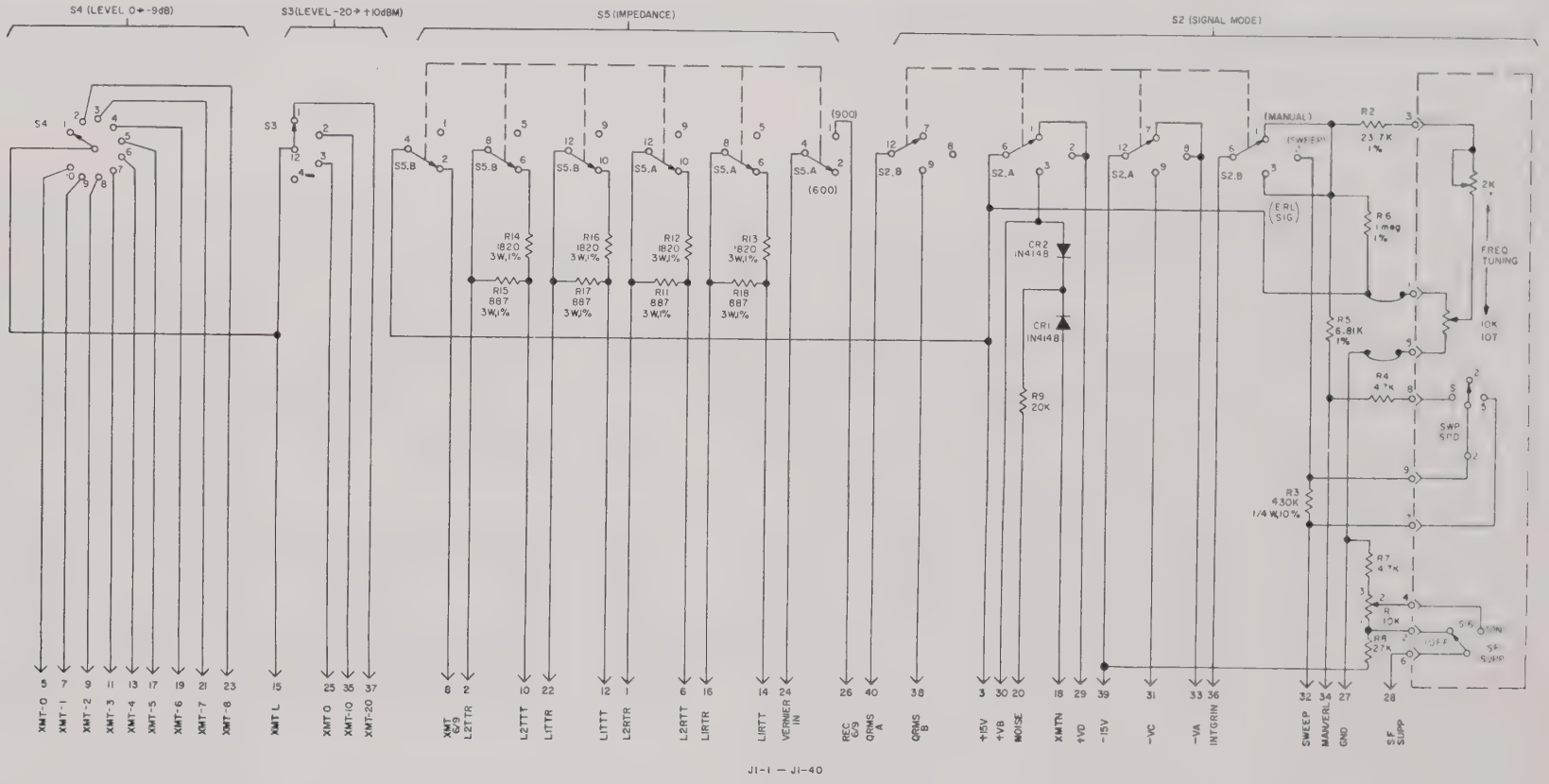
WIRE NO.	COLOR	GA	APPROX LENGTH	SIGNAL NAME	FROM	NOTES	TO	NOTES
A5.W1	WHT/RED/BLK			MARKER	A5.1		A7.8	
A5.W2	WHT/RED/GRN			INTEN	A5.2	LOCATED ON A15	A7.5	
A5.W3	WHT/RED/BRN			HORIZ	A5.4		A7.3	
A5.W4	WHT/RED/ORN			VERT	A5.3		A7.6	
A5.W5	GRN			GND	A5.5		A7.7	
A15.W28	RED			+5	S11.2		A7.15	
A15.W29	GRN			GND	S10.2		A7.18	
A15.W30	WHT/BLK			DSP (A)	S10.3		A7.14	
A15.W31	WHT/BRN			DISP (B)	S10.1		A7.17	
A15.W32	WHT/RED			CLR (B)	S12.1		A7.12	
A15.W33	WHT/ORN			NORM (A)	S12.3		A7.6	
A15.W34	WHT/YEL			CLR (B)	S11.1		A7.13	
A15.W35	WHT/GRN			NORM (B)	S11.3		A7.11	
A15.W36	WHT/BLU			X 1/4 (A)	S13.1		A7.10	
A15.W37	WHT/PRP			X 1/4 (B)	S13.2		A7.9	

Figure 7—2. Level Tracer Assembly (Sheet 2)



Transmit Control Switch	
NE PART NO.	B8100-00-010
REF DESIG	A1
PC NO.	96734

Figure 7—3. Transmit Control Switch A1, Parts Location Diagram



NOTES

1 UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS

Figure 7—4. Transmit Control Switch A1, Schematic Diagram

SECTION 7

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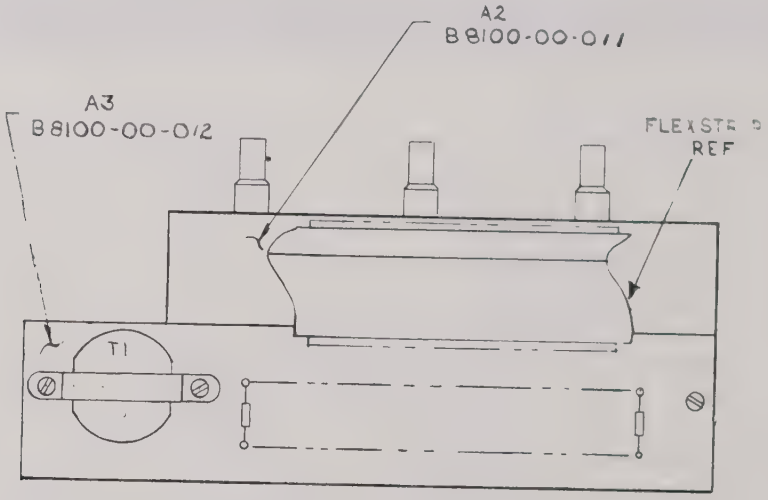
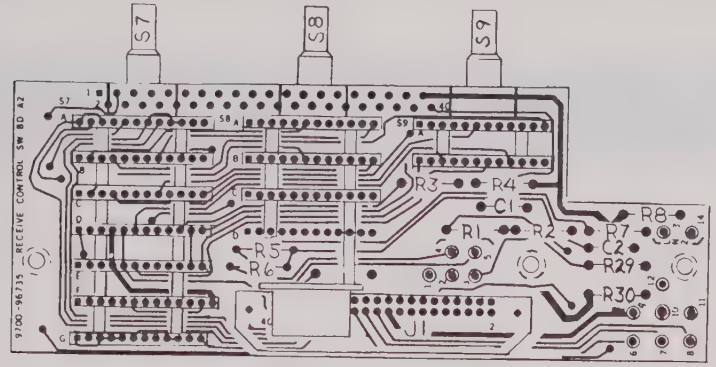
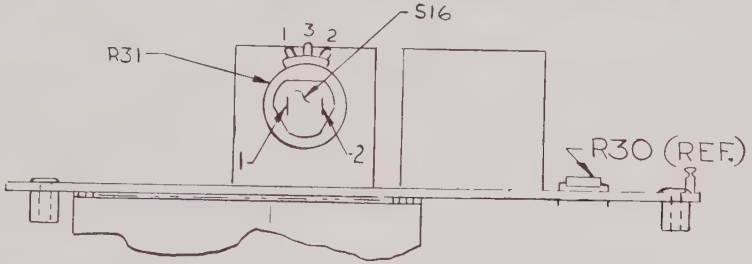


WIRE LIST		
FROM	TO	COLOR
T1	A3. 8	YELLOW
T1	A3. 9	YEL/WHT.
T1	A3. 13	ORANGE
T1	A3. 12	BLACK
T1	A3. 5	OR/WHT
T1	A3. 11	BLUE
T1	A3. 14	BRN/WHT
T1	A3. 1	BROWN
T1	A3. 4	RED/WHT
T1	A3. 10	RED

Receive Control Switch	
NE PART NO	8100-00-023
REF DESIG	A13
PC NO	

Figure 7—5. Receive Control Switch A13, Parts Location Diagram

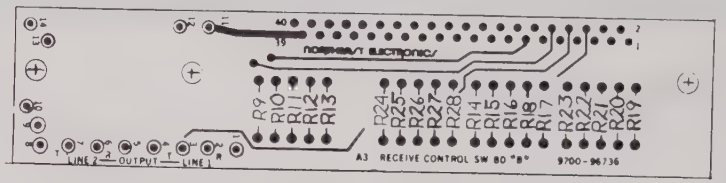




WIRE LIST			
FROM	TO	AWG	COLOR
R31.1	2	24	WHT/TEFLON
R31.2	3	24	WHT/TEFLON
R31.3	1	24	WHT/TEFLON
S16.1	11	24	WHT/TEFLON
S16.2	12	24	WHT/TEFLON

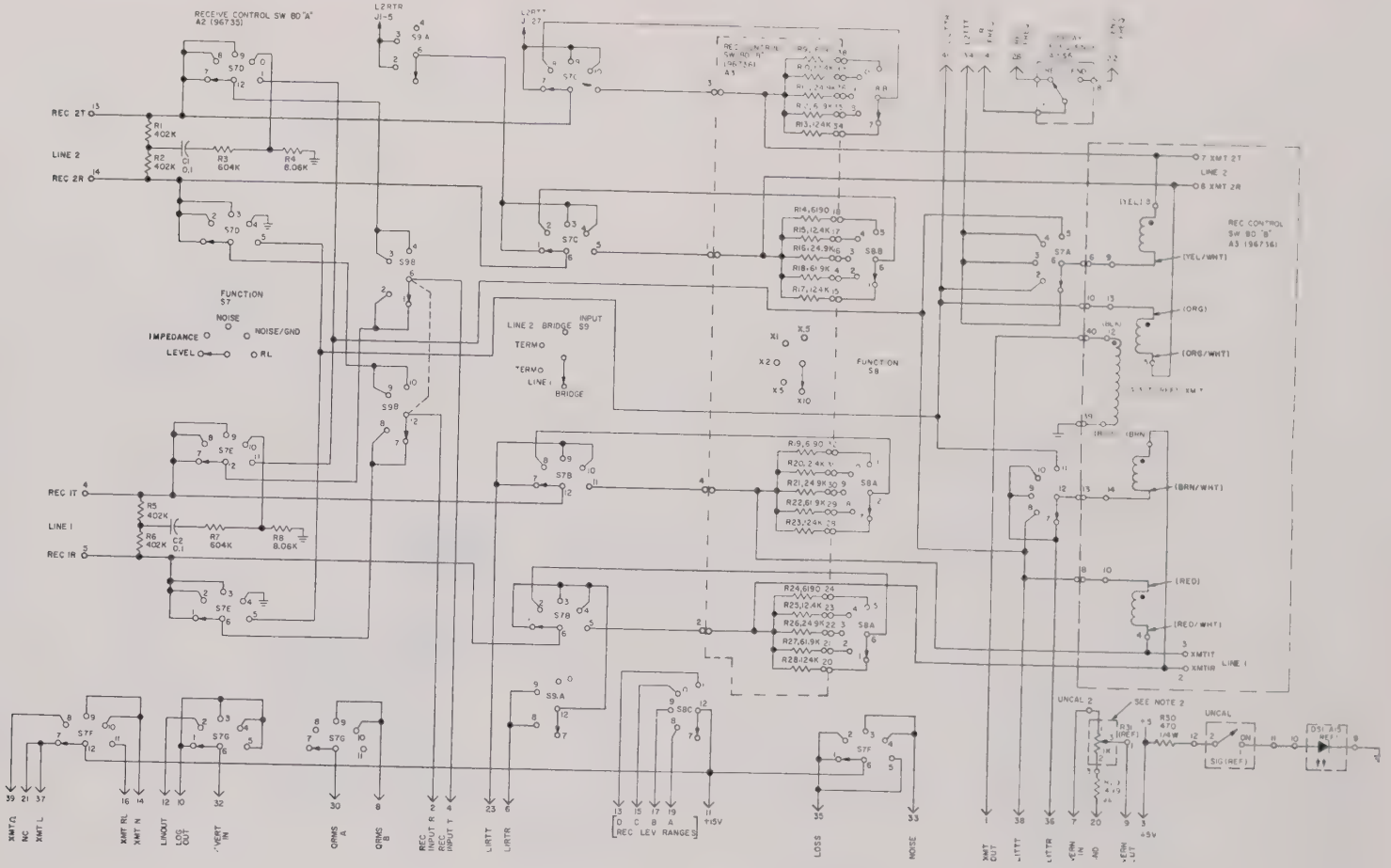
"A" Receive Control Switch	
NE PART NO	B8100-00-011
REF DESIG	A2
PC NO	96735

Figure 7—6. "A" Receive Control Switch A2, Parts Location Diagram



"B" Receive Control Switch	
NE PART NO.	B8100-00-012
REF DESIG	A3
PC NO.	96736

Figure 7—7. "B" Receive Control Switch A3, Parts Location Diagram



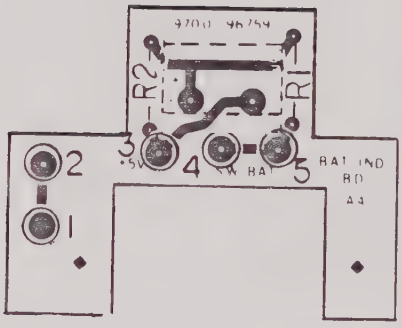
NOTES:

2. R31 AND SWITCH S16 MOUNTED ON SWITCH S8.

1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE EXPRESSED IN OHMS
   CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS

HIGHEST REFERENCE DESIGNATIONS	
R30	C2
S9	J1

Figure 7—8. Receive Control Switch A13, Schematic Diagram



Battery Indicator	
NE PART NO.	B8100-00-013
REF DESIG	A4
PC NO.	96759

Figure 7—9. Battery Indicator A4, Parts Location Diagram

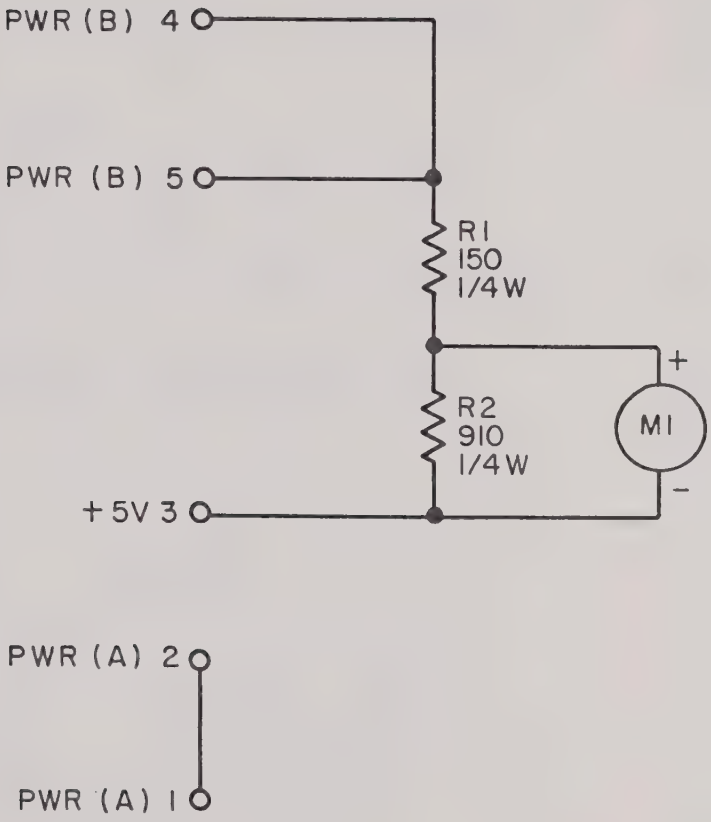


Figure 7—10. Battery Indicator A4, Schematic Diagram

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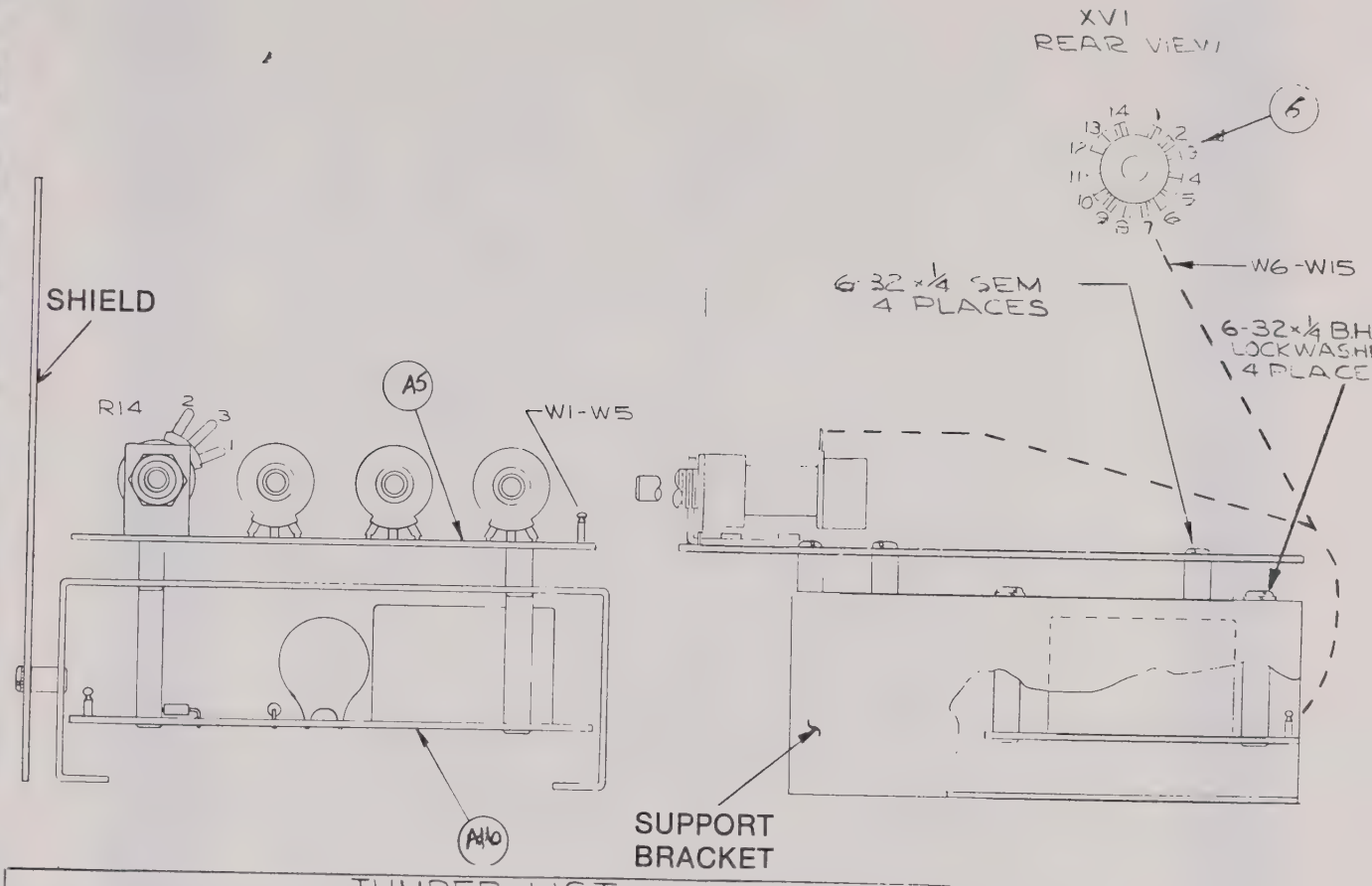
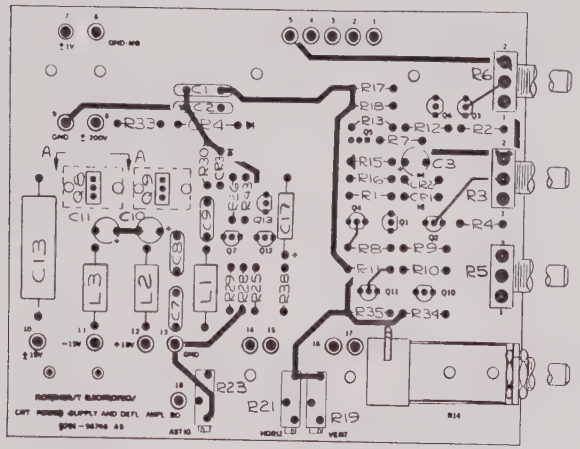


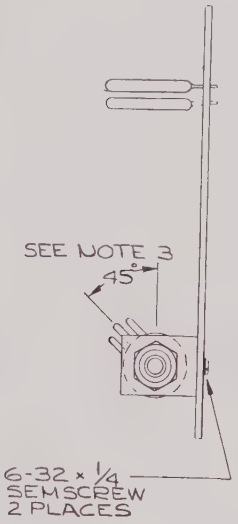
JUMPER LIST

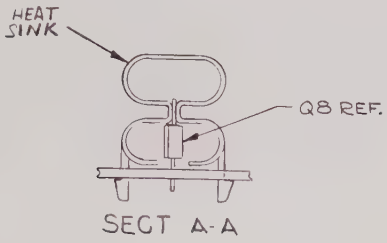
WIRE NO	COLOR	GA	APPROX LENGTH	SIGNAL NAME	FROM	NOTES	TO	NOTES
W1	WHT/RED/BLK	22 STR	12"	MARKER	A5.1		FEM Q.D.	W1-W5
W2	WHT/RED/BRN	"	12"	INTEN	A5.2		FEM Q.D.	TO BE CONNECTED TO A7 AT 001 LEVEL
W3	WHT/RED/RED	"	12"	HORIZ	A5.4		FEM Q.D.	
W4	WHT/RED/ORN	"	12"	VERT	A5.3		FEM Q.D.	
W5	GRN	"	12"	GND(MB)	A5.5		FEM Q.D.	
W6	BLK	"	18"	ASTIG	A5.18		XVI.9	
W7	BRN	"	18"	HOR PLATE(A)	A5.14		XVI.4	TWISTED PAIR
W8	YEL	"	18"	HOR PLATE(B)	A5.15		XVI.6	
W9	SLT	"	18"	VERT PLATE(A)	A5.16		XVI.10	TWISTED PAIR
W10	WHT	"	18"	VERT PLATE(B)	A5.17		XVI.12	
W11	RED	18 STR	18"	FOCUS	A5.R14 PIN 3		XVI.2	
W12		18 STR	18"	CATHODE	A16.6		XVI.7	
W13		18 STR	18"	GRID	A16.5		XVI.3	
W14		18 STR	18"	FILAMENT	A16.8		XVI.14	BELDEN #8899
W15		18 STR	18"	-2KV	A16.7		XVI.1	
W16		18 STR	9"	-1724V	A5.R14 PIN 1		A16.1	
W17	RED	18 STR	9"	-1590V	A5.R14 PIN 2		A16.2	
W18	WHT/BLK	22 STR	9"	±1V	A5.7	FEM Q.D.	A16.4	
W19	WHT/BRN	22 STR	6"	±200	A5.8	FEM Q.D.	A 6.10	
W20	WHT/RED	22 STR	6"	GND	A5.9	FEM Q.D.	A16.11	
W21	WHT/ORN	22 STR	6"	±15V	A5.10	FEM Q.D.	A16.9	
W22	WHT/YEL	22 STR	6"	GND(MB)	A5.6	FEM Q.D.	A16.3	

High Voltage	
NE PART NO.	C8100-00-027
REF DESIG	A14
PC NO.	

Figure 7—11. High Voltage A14, Parts Location Diagram



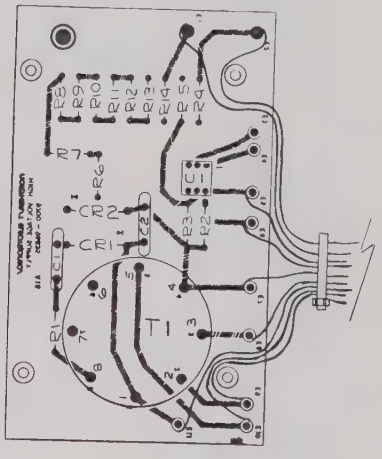




1⊙ DENOTES MALE QUICK DISCONNECTS LOCATED 18 PLACES

CRT Power Supply And Deflection Amplifier	
NE PART NO.	B8100-00-029
REF DESIG	A5
PC NO.	96746

Figure 7—12. CRT Power Supply And Deflection Amplifier A5, Parts Location Diagram



1⊙ DENOTES MALE QUICK DISCONNECTS

Figure 7—13. High Voltage Supply A16, Parts Location Diagram

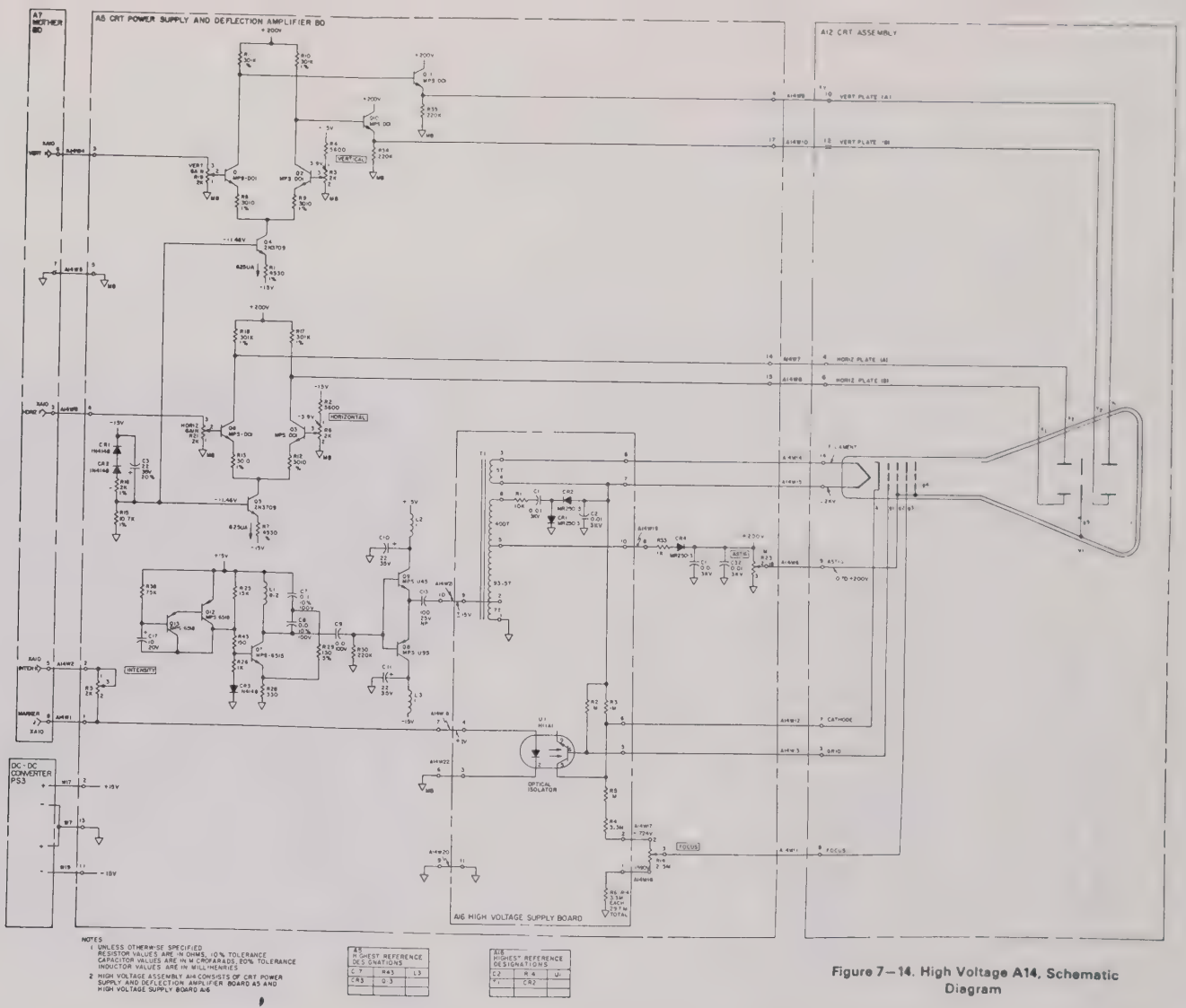
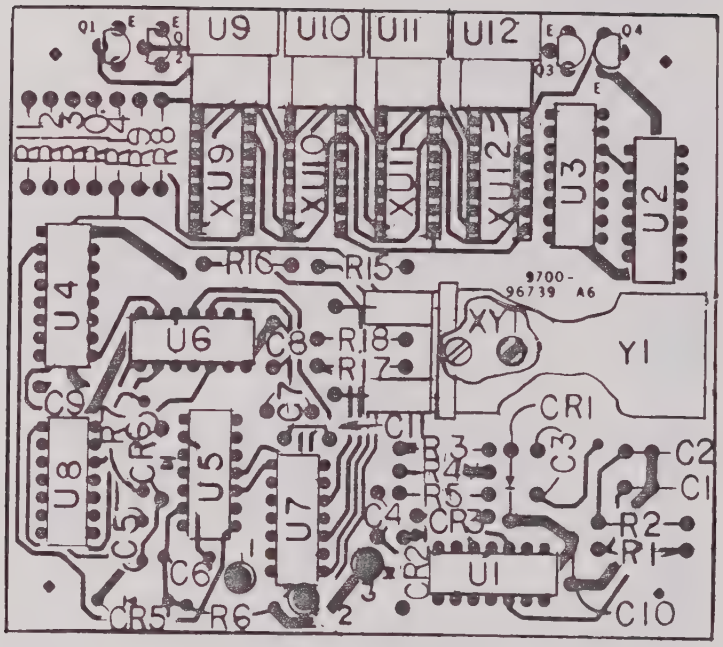
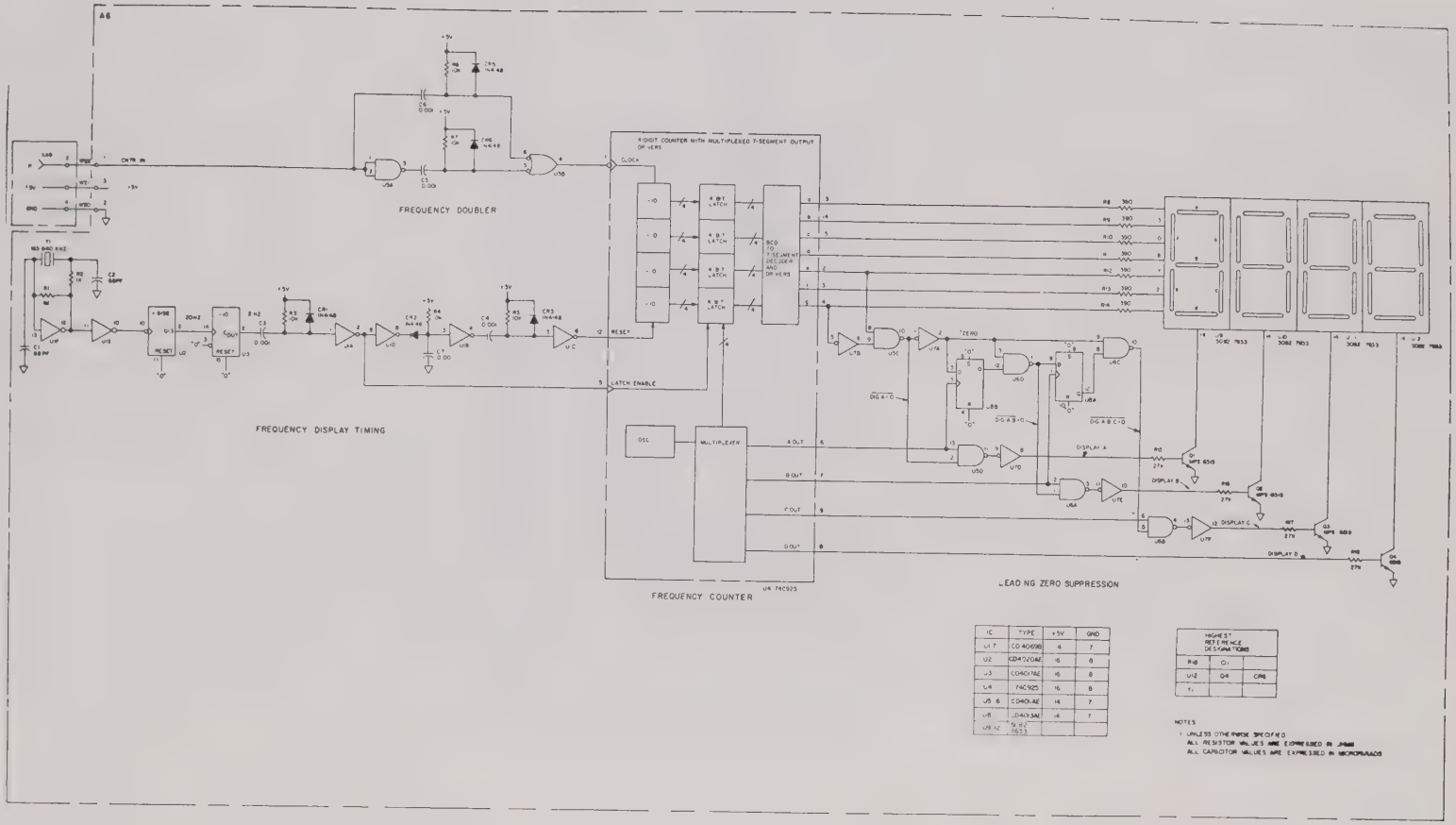


Figure 7—14. High Voltage A14, Schematic Diagram



Frequency Counter And Display	
NE PART NO.	B8100-00-015
REF DESIG	A6
PC NO.	96739

Figure 7—15. Frequency Counter And Display A6, Parts Location Diagram

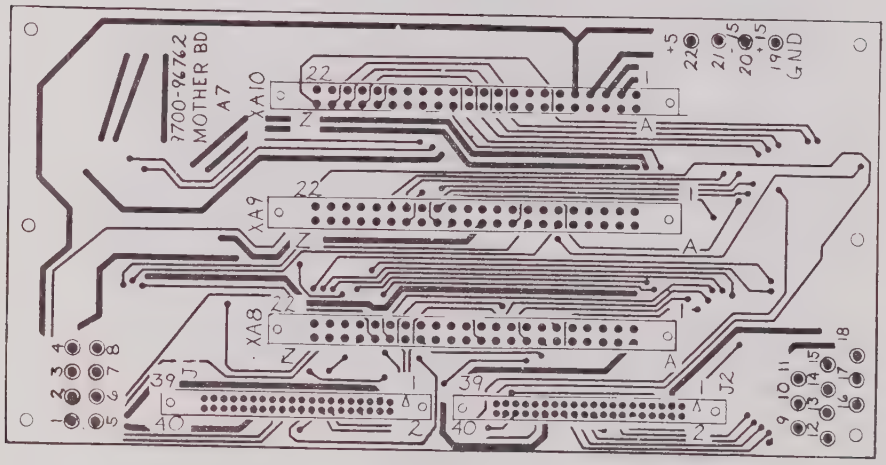


IC	TYPE	+5V	GND
U1,7	CD 4069UB	4	7
U2	ICM7320AE	16	8
U3	LD4047AE	16	8
U4	F4C925	16	8
U5,6	CD4011AE	14	7
U8	LD4013AE	14	7
U9,10	SN 8DZ 7853		

HIGHEST REFERENCE DESIGNATORS		
R48	C1	
U12	Q4	CR8
Y1		

NOTES
1. UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE EXPRESSED IN OHMS
ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS

Figure 7—16. Frequency Counter And Display A6, Schematic Diagram



Mother Board	
NE PART NO.	C8100-00-016
REF DESIG	A7
PC NO.	96762

Figure 7—17. Mother Board A7, Parts Location Diagram

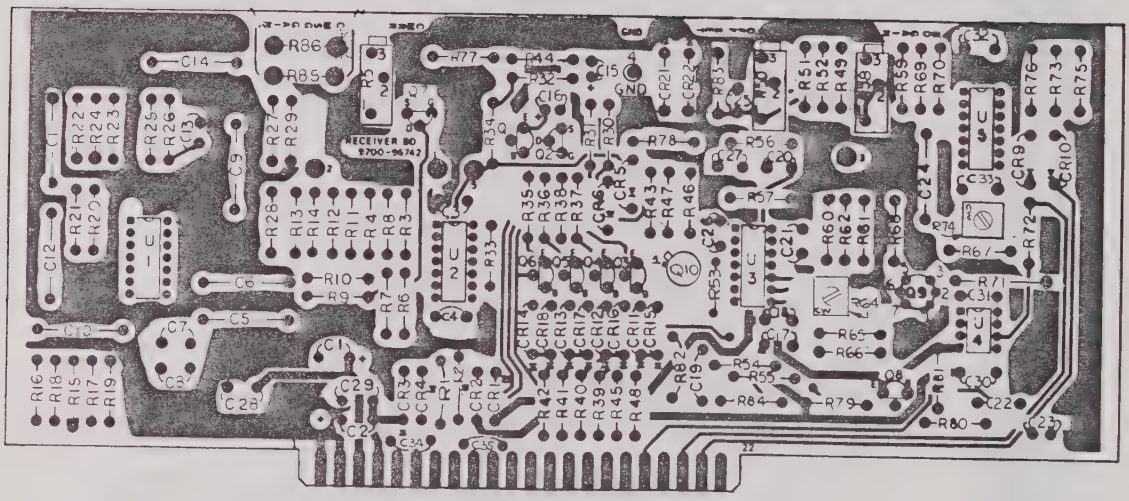
SIGNAL	STATION	STATION
GND	4	XA10.2
	XA10.2	XA10.B
	XA10.B	XA9.2
	XA9.2	XA9.B
	XA9.B	XA8.2
	XA8.2	XA8.B
	XA8.B	18
	18	J2.20
	J2.20	J1.27
	J1.27	4
GND	4	7
+5V	22	XA10.5
	XA10.5	XA10.E
	XA10.E	XA9.5
	XA9.5	XA9.E
	XA9.E	15
	15	J2.3
+5V	J2.3	1
-15V	21	XA10.4
	XA10.4	XA10.D
	XA10.D	XA9.4
	XA9.4	XA9.D
	XA9.D	XA8.4
	XA8.4	XA8.D
-15V	XA8.D	J1.39
+15V	20	XA10.3
	XA10.3	XA10.C
	XA10.C	XA9.3
	XA9.3	XA9.C
	XA9.C	XA8.3
	XA8.3	XA8.C
	XA8.C	J2.11
+15V	J2.11	J1.3

SIGNAL	STATION	STATION
-VC	XA9.1	J1.29
+VB	XA9..	J1.30
-Vc	XA9.M	J1.31
-VA	XA9.A	J1.33
CNTR IN	2	XA9.P
LOSS	XA8.9	J2.35
NOISE	XA8.6	J2.33
RECEIVE LEVEL RANGES A	XA8.S	J2.19
RECEIVE LEVEL RANGES B	XA8.R	J2.17
RECEIVE LEVEL RANGES C	XA8.P	J2.15
RECEIVE LEVEL RANGES D	XA8.N	J2.13
REC. INPUT T	XA8.H	J2.4
REC. INPUT R	XA8.J	J2.2
QRMS A	XA8.1	XA8.A
|	XA8.A	J2.30
|	J2.30	J1.40
QRMS B	XA8.U	J2.8
|	J2.8	J1.38
VERNIER IN	XA8.V	J1.24
|	J1.24	J2.7
REC 6/9	XA8.W	J1.26
VERNIER OUT	XA8.X	J2.9
LIN OUT	XA8.Y	J2.12
LOG OUT	XA8.21	J2.10
VERT IN	XA10.P	J2.32
x1/4A	XA8.20	10
x1/4 B	XA8.18	9
REC FREQ	XA8.M	J2.26
SND FREQ	XA9.K	J2.22
S/R FREQ	XA9.R	J2.24
SWEEP	XA9.8	J1.32
INTGR IN	XA9.F	J1.36
MAN/ERL	XA9.J	J1.34

SIGNAL	STATION	STATION
SF SUPP.	XA9.H	J1.28
XMT N	XA9.17	J2.14
XMT N	J2.14	J1.18
XMT RL	XA9.16	J2.16
XMT L	J2.37	J1.15
XMT ⊓	J2.39	XA9.22
XMT ⊓	XA9.22	XA8.Z
XMT -20	XA9.T	J1.37
XMT -10	XA9.15	J1.35
XMT 0	XA9.S	J1.25
XMT -8	XA9.Z	J1.23
XMT -7	XA9.21	J1.21
XMT -6	XA9.Y	J1.19
XMT -5	XA9.20	J1.17
XMT -4	XA9.X	J1.13
XMT -3	XA9.19	J1.11
XMT -2	XA9.W	J1.9
XMT -1	XA9.18	J1.7
XMT -0	XA9.V	J1.5
XMT 6/9	XA9.U	J1.8
XMT OUT	XA9.14	J2.1
ERL FIL IN	XA9.9	XA9.L
F/	XA9.N	XA10.S
CLR A	XA10.W	12
CLR B	XA10.X	13
DISP A	XA10.Y	14
DISP B	XA10.Z	17
ACTIVE A	XA10.U	16
ACTIVE B	XA10.V	11
NOISE	XA10.T	J1.20
VERT	XA10.1	6
HORIZ	XA10.F	3
INTEN	XA10.K	5
MARKER	XA10.J	8

SIGNAL	STATION	STATION
L1 RTT	J1.14	J2.23
L1 RTR	J1.16	J2.6
L2 RTT	J1.6	J2.27
L2 RTR	J1.1	J2.5
L1 TTT	J1.12	J2.38
L1 TTR	J1.22	J2.36
L2 TTT	J1.10	J2.34
L2 TTR	J1.2	J2.40

Figure 7—18. Mother Board A7, Schematic Diagram



Receiver	
NE PART NO.	C8100-00-017
REF DESIG	A8
PC NO.	96742

Figure 7—19. Receiver A8, Parts Location Diagram

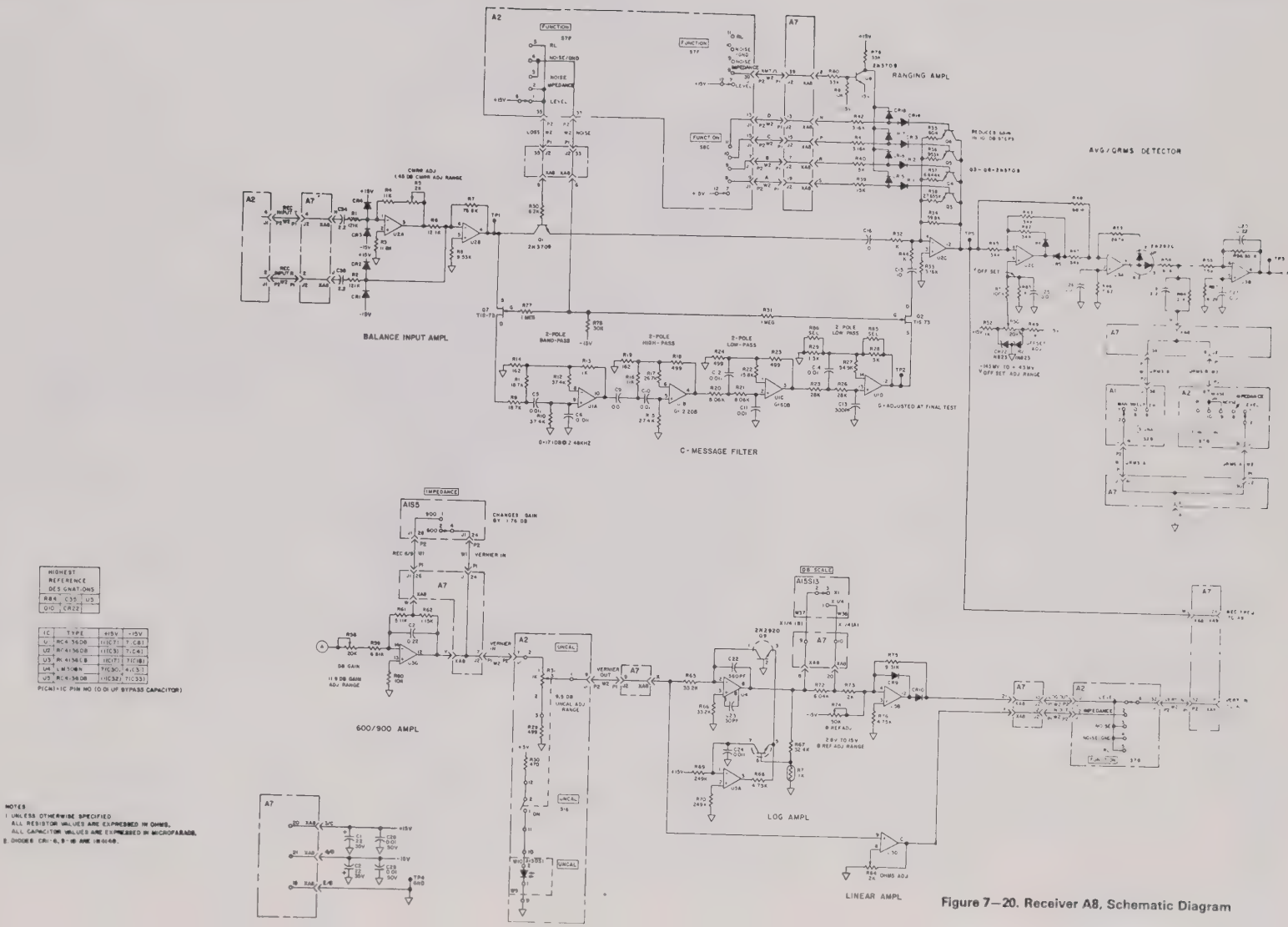
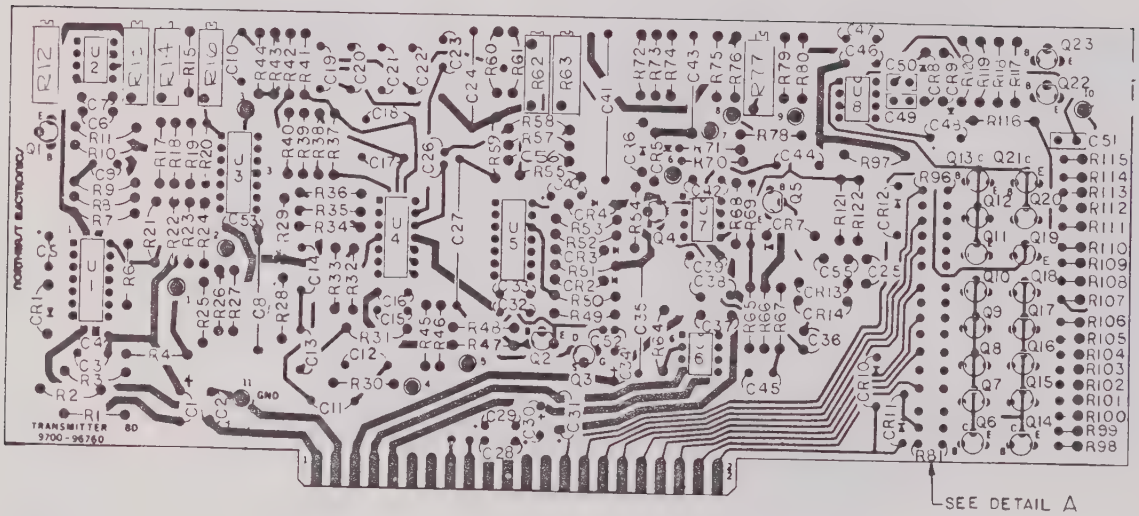
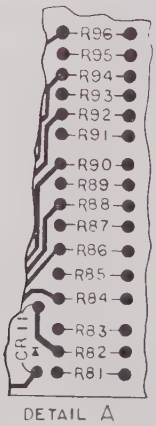


Figure 7—20. Receiver A8, Schematic Diagram





DETAIL A

Transmitter	
NE PART NO.	C8100-00-018
REF DESIG	A9
PC NO.	96760

Figure 7—21. Transmitter A9, Parts Location Diagram

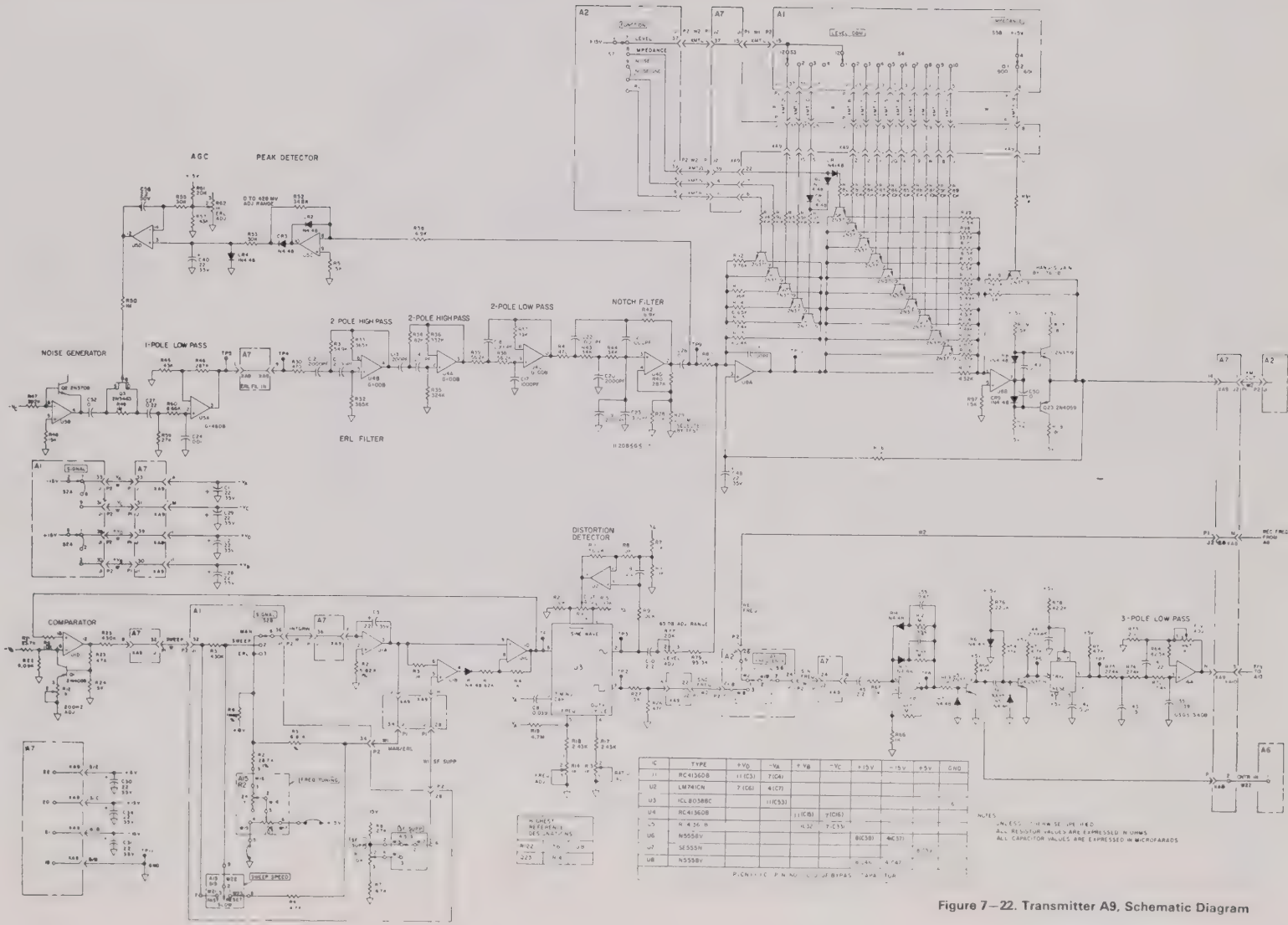
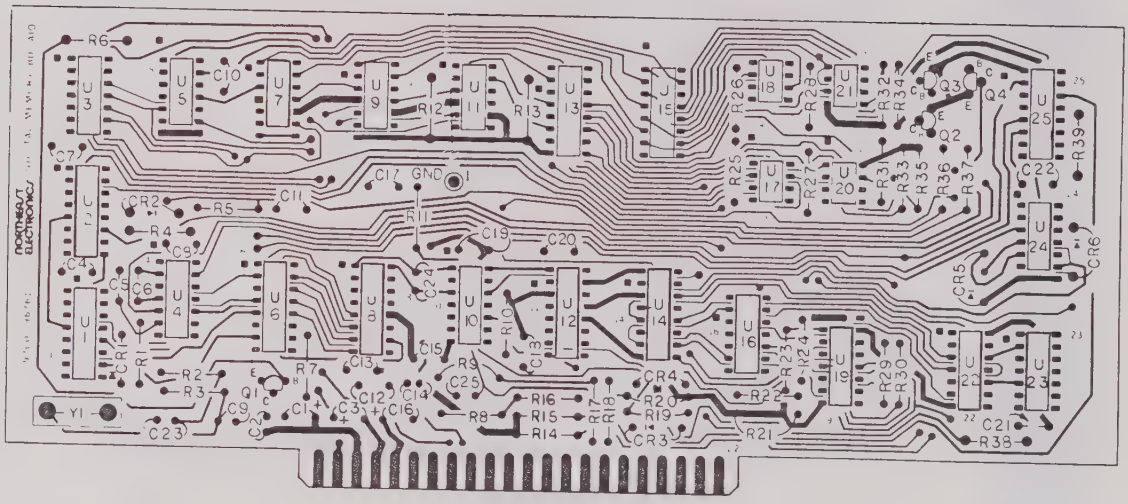
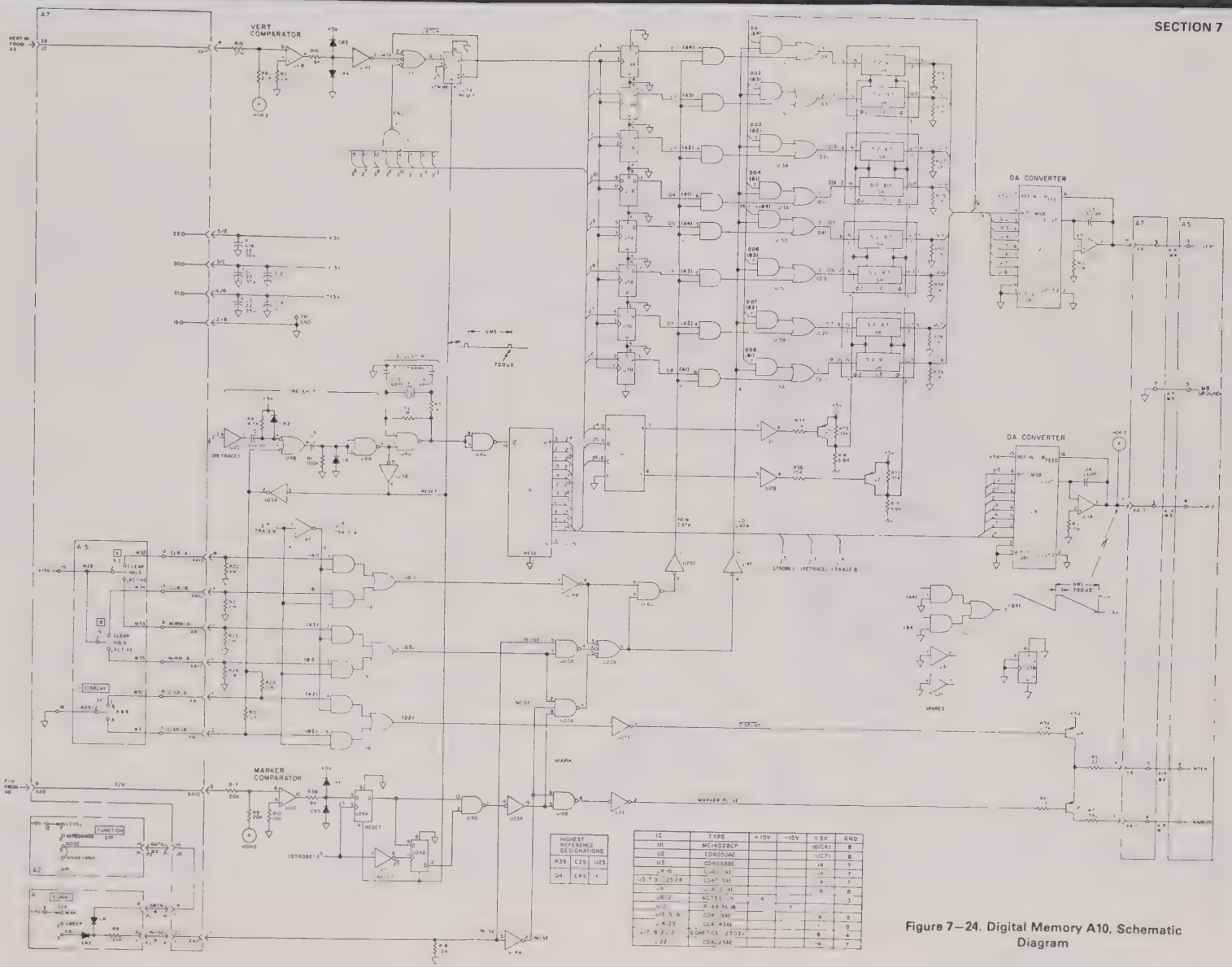


Figure 7–22. Transmitter A9, Schematic Diagram



Digital Memory	
NE PART NO.	C8100-00-019
REF DESIG	A10
PC NO.	96761

Figure 7—23. Digital Memory A10, Parts Location Diagram

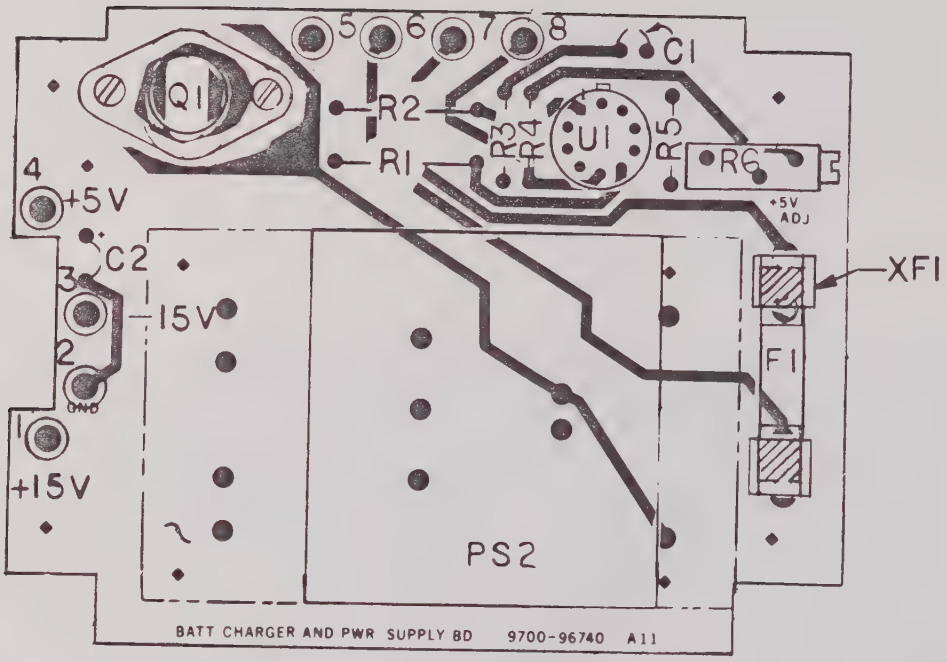


NOTES
- UNLESS OTHERWISE SPECIFIED
- ALL RESISTOR VALUES ARE EXPRESSED IN OHMS
- ALL CAPACITOR VALUES ARE EXPRESSED AS MICROFARADS
- ALL DIODES ARE 1N4148
- TRANSISTORS Q1 THROUGH Q8 ARE 2N4058

HIGHEST REFERENCE DESIGNATIONS		
R39	C25	U25
Q4	CR6	Y

IC	TYPE	+15V	-15V	+5V	GND
U1	MC14028CP			16(C4)	8
U2	CD4050AE			1(C7)	8
U3	CD4068BE			14	7
U4,16	CD4 AE			16	7
U5,7,9, 23,24	CD40 3AE			4	7
U6	CD 4 2 AE			6	8
U8,12	MC1553 JL	4			5
U10	R 44 35 JB		7		
U13,15,19	CD4 9AE			6	8
U14,23	CD4 43AE			1	8
U17,18,21,22	SIGNETICS 2503			8	4
U20	CD4 03AE			14	7

Figure 7–24. Digital Memory A10, Schematic Diagram



Power Supply	
NE PART NO.	B8100-00-020
REF DESIG	A11
PC NO.	96740

Figure 7—25. Power Supply A11, Parts Location Diagram

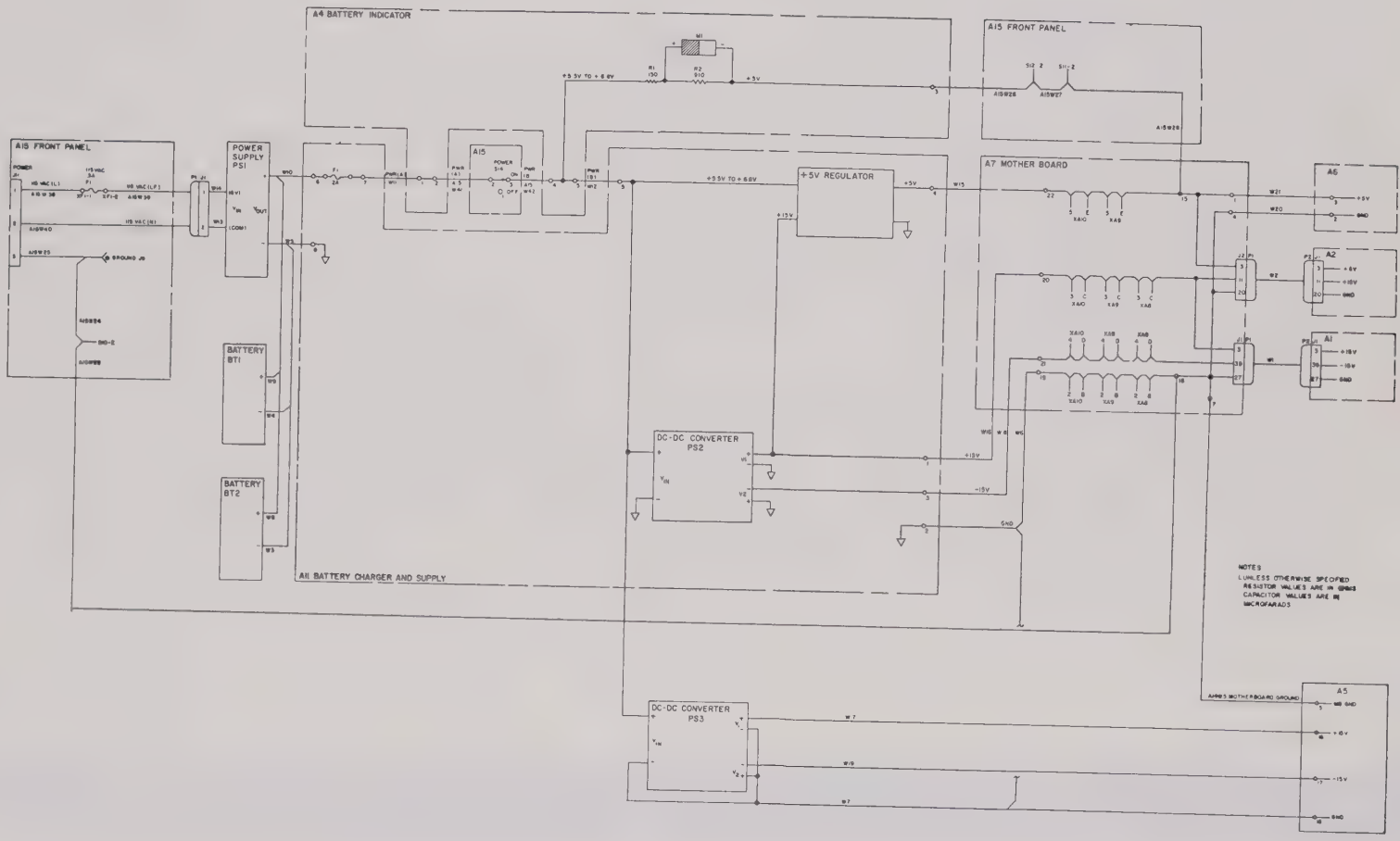
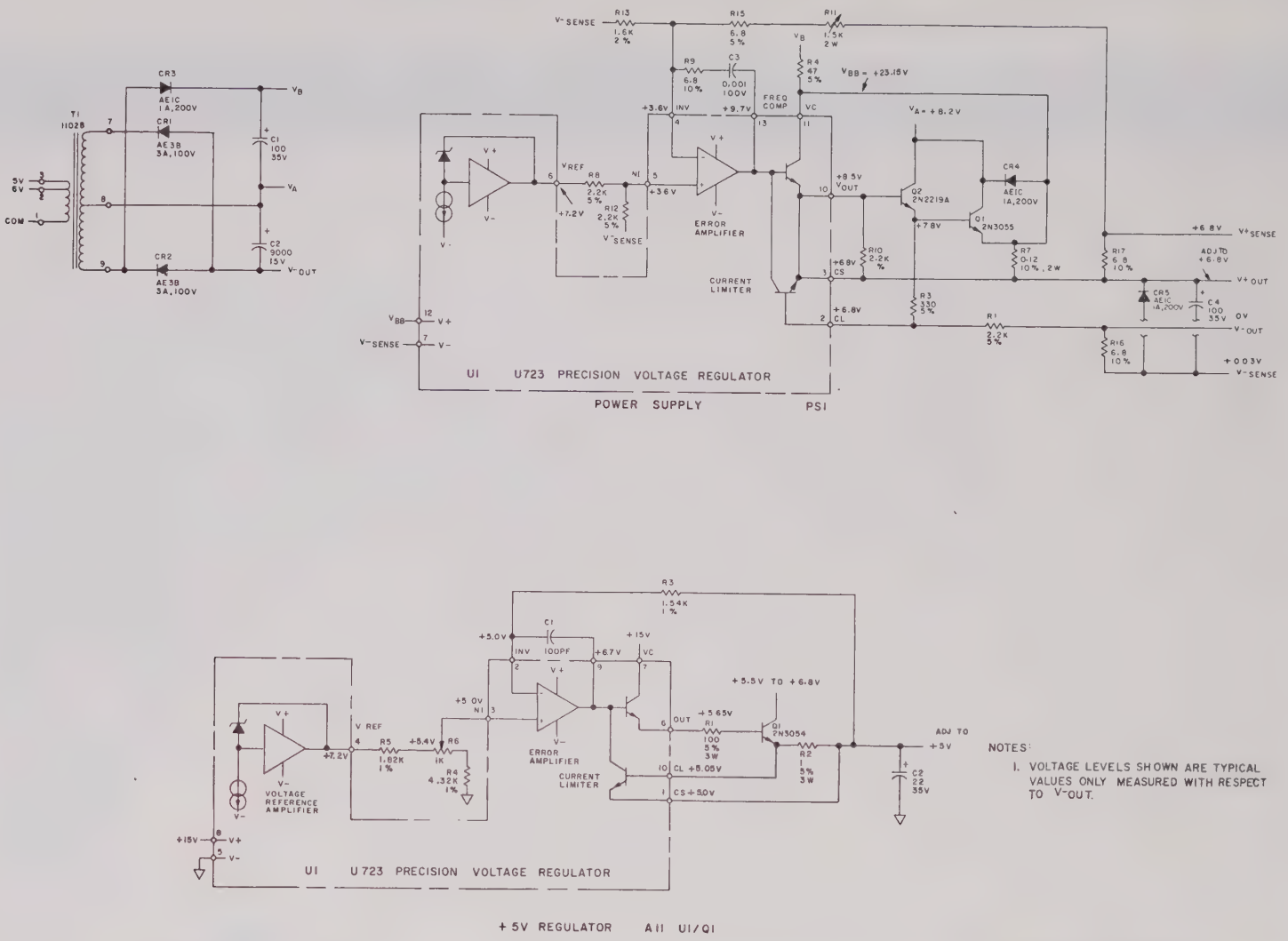


Figure 7—26. Power Supply A11, Schematic Diagram (Sheet 1)



NOTES:

1. VOLTAGE LEVELS SHOWN ARE TYPICAL VALUES ONLY MEASURED WITH RESPECT TO V-OUT.

Figure 7–26. Power Supply A11, Schematic Diagram (Sheet 2)

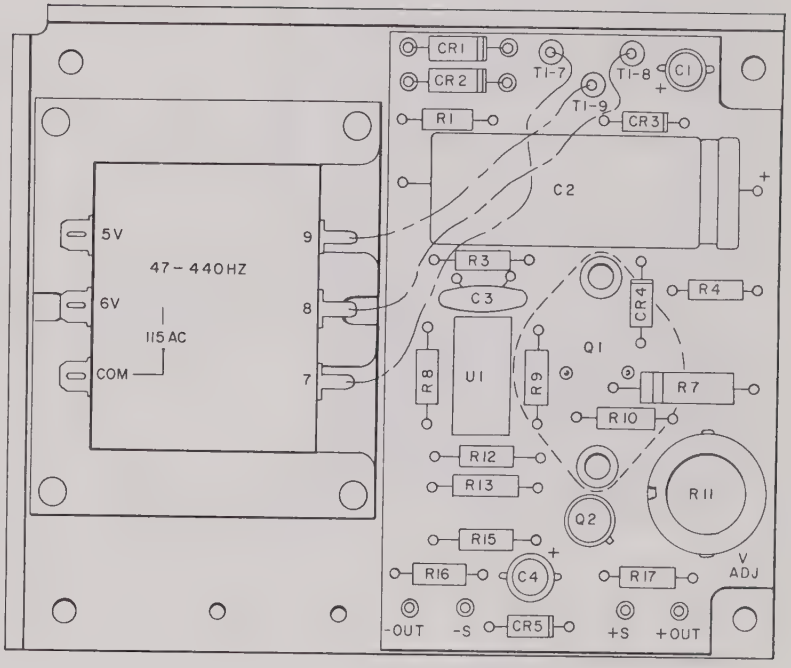
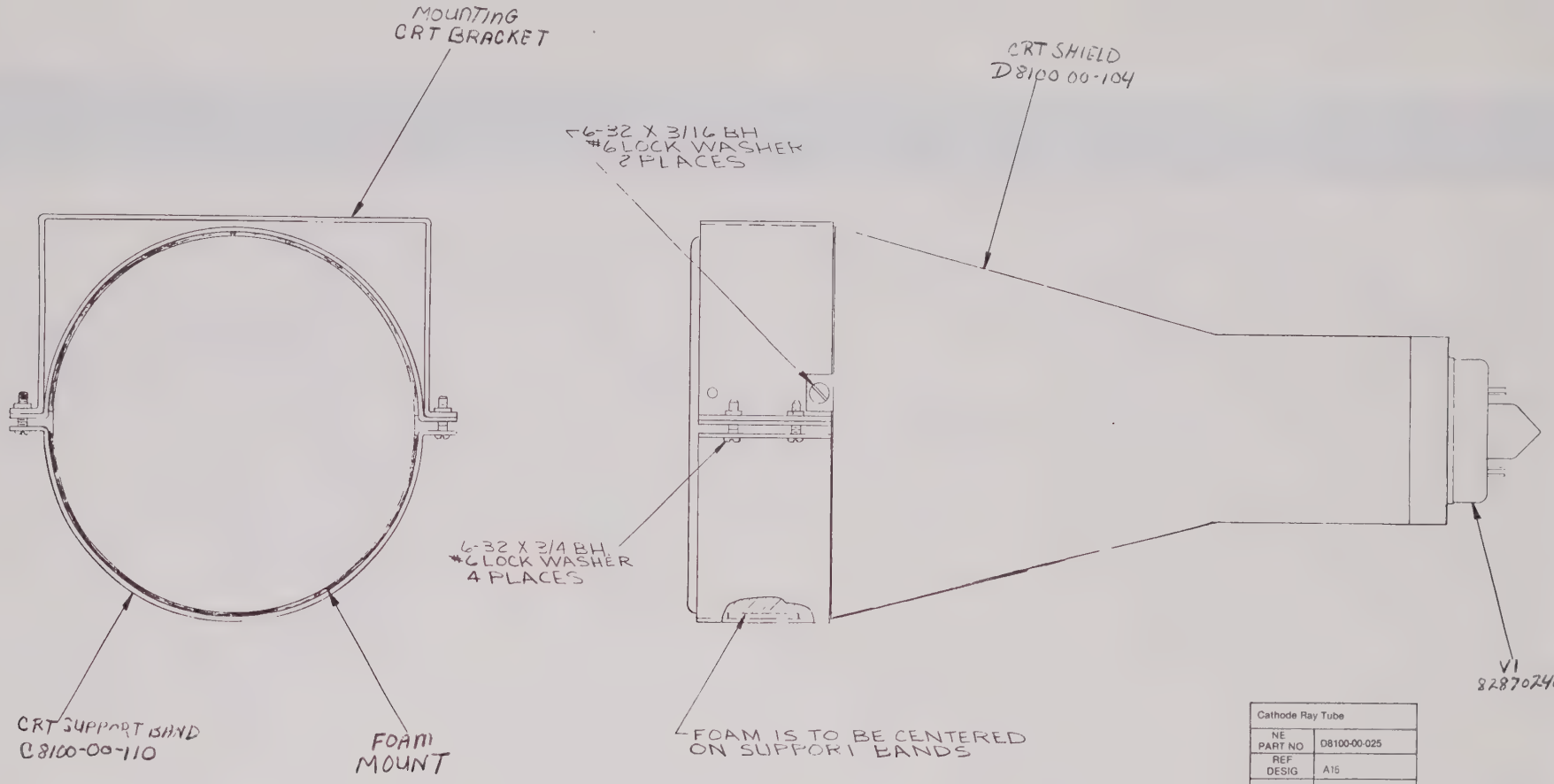
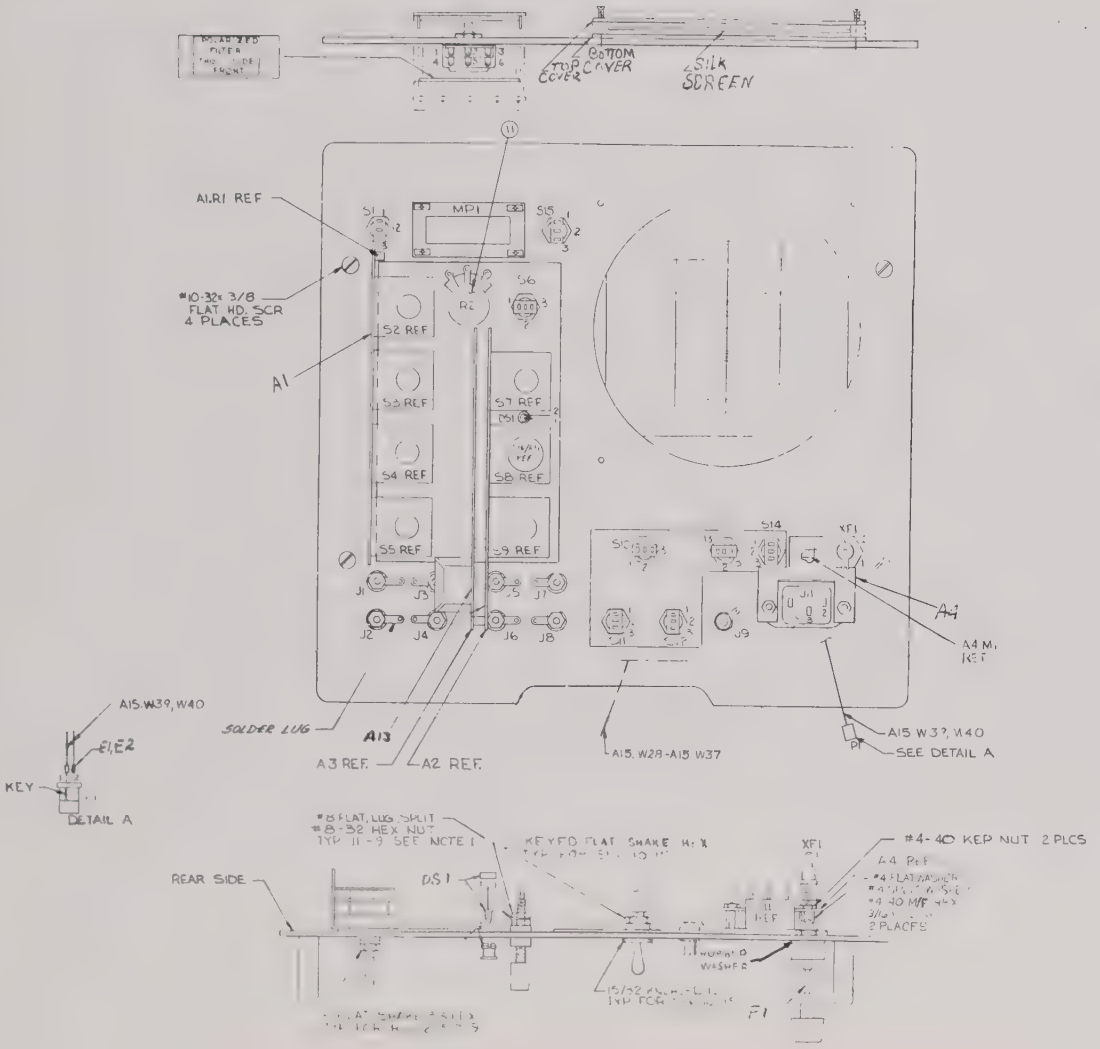


Figure 7–27. Power Supply A11PS1 Parts Location Diagram



Cathode Ray Tube	
NE PART NO	D8100-00-025
REF DESIG	A15
PC NO	

Figure 7—28. Cathode Ray Tube A12



JUMPER LIST

WIRE NO.	COLOR	GA	APPROX LENGTH	SIGNAL NAME	FROM	NOTES	TO	NOTES
W1	WHT/RED	24	3"	XMT2R	J2	TWISTED PAIR	A3,7	
W2			3"	XMT2R	J2		A3,8	
W3			3"	XMT1R	J3	TWISTED PAIR	A3,3	
W4			3"	XMT1R	J4		A3,2	
W5			3"	REC2T	J5	TWISTED PAIR	A2,3	
W6			3"	REC2R	J6		A2,4	
W7			5"	REC1T	J7	TWISTED PAIR	A2,4	
W8			5"	REC1R	J8		A2,5	
W9			6"	DS1(-)	DS1,1		A2,9	
W10			6"	DS1(+)	DS1,2		A2,10	
W11			3"	SFSWON	S1,3		A1,4	
W12			3"	SFSWCOM	S1,2		A1,6	
W13			3"	SFSWOFF	S1,1		A1,2	
W14			1"	STRAP	R2,2		R2,5	
W15			3"	FREQADJ1	R2,4		A1,5	
W16			3"	FREQADJ2	R2,3		A1,3	
W17			3"	FREQADJ3	R2,6		A1,1	
W18			9"	DISPREQGND	S6,3		A2,5	
W19			9"	DISPREQCOM	S6,2		A2,7	
W20			9"	DISPREQREC	S6,1		A2,6	
W21			6"	SWP FAST	S15,3		A1,7	
W22			6"	SWP SLOW	S15,2		A1,9	
W23	WHT/YELLOW	24	6"	RESET SWP	S15,1		A1,8	
W24	BRN	22STR	3"	GND	S10,2		J9	
W25	GRN	22STR	4"	GND	J9		J1,3	
W26	RED	22STR	4"	+5V	A4,3		S12,2	
W27	RED	22STR	3"	+5V	S12,2		S11,2	
W28	RED	22STR	12"	+5V	S11,2		FEM,Q,D	
W29	GRN	22STR	12"	GND	S10,2		FEM,Q,D	
W30	WHT/BLK	22STR	12"	DISP (A)	S10,3		FEM,Q,D	
W31	WHT/BRN	22STR	12"	DISP (B)	S10,1		FEM,Q,D	W28 W17
W32	WHT/RED	22STR	12"	CLR (A)	S12,1		FEM,Q,D	TO BE CONNECTED TO
W33	WHT/ORN	22STR	12"	NORM (A)	S12,3		FEM,Q,D	CONNECTED TO
W34	WHT/YEL	22STR	12"	CLR (B)	S11,-		FEM,Q,D	A17 AT 0DB
W35	WHT/GRN	22STR	12"	NORM (B)	S11,3		FEM,Q,D	LEVEL
W36	WHT/BLU	22STR	12"	λ 1/4 (A)	S13,1		FEM,Q,D	
W37	WHT/PRP	22STR	12"	λ 1/4 (B)	S13,2		FEM,Q,D	
W38	BLK	18STR	4"	110 VAC (L)	J11,1		XF1,1	
W39	BLK	18STR	6"	110 VAC (L1)	XF1,2		P1,1	
W40	WHT	18STR	4"	110 VAC (N)	J11,2		P1,2	
W41	SLT	22STR	2"	PWR (A)	S14,2		A4,2	
W42	BRN	22STR	3"	PWR (B)	S14,3		A4,4	

Twist pair

Front Panel	
NE PART NO.	D8100-00-026
REF DESIG	A15
PC NO	

Figure 7—29. Front Panel A15

SECTION 8

PARTS LIST

8.1 This section contains parts lists for electronic components in the Model 8100 Level Tracer. The assembly diagrams and parts location diagrams in Section 7 show where individual parts are used within the Level Tracer.

Table 8—1. Level Tracer Overall Assembly

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
BT1-2	BATTERY,LEAD-CALCIUM				GLOBE	G0680-1,TYPE B	91000103
MP1	COVER ASSY						D810000298
MP2	CASE ASSY						D810000299
W1	PWR. CORD, 7½' YEL. 3 COND				BELDEN	17250	932000801

Table 8—2. Level Tracer Assembly

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
J1	2 COND				AMP	1-480319-0	650900100
PS1	POWER SUPPLY 115 VAC INPT				POWER ONE	B5-3.0	960101801
W1-2	CABLE ASSY W1-2						A810000024

Table 8—3. Transmit Control Switch A1

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
CR1-2	DO35 4NS 10MA SI 50UA				FAIRCHILD	1N4148	560041460
J1	40 PIN				3M	3432-1002	654001901
R1	10K	.75W	10%		HELIPOT	89PR10K	232501030
R2	23.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223721
R3	430K	1/4W	10%		AB	TYPE CB	200104346
R4	4.7K	1/4W	10%		AB	TYPE CB	200104726
R5	6810-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220268111
R6	1M	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210041
R7	4.7K	1/4W	10%		AB	TYPE CB	200104726
R8	27K	1/4W	10%		AB	TYPE CB	200102736
R9	20K	1/4W	5%		AB	TYPE CB	200102035
R10	3.3K	1/4W	10%		AB	TYPE CB	200103326
R11	887-	3W	1%		TEL LABS	EL3	200988701
R12-14	1820-	3W	1%		TEL LABS	EL3	200918211
R15	887-	3W	1%		TEL LABS	EL3	200988701
R16	1820-	3W	1%		TEL LABS	EL3	200918211
R17-18	887-	3W	1%		TEL LABS	EL3	200988701
S2	PC BD MTG				LEDEX	753519-001	625000401
S3	PC BD MTG				LEDEX	753521-001	625000403
S4	PC BD MTG				LEDEX	753522-001	625000404
S5	PC BD MTG				LEDEX	753524-001	625000406

Table 8—4. Receive Control Switch A13

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
A2	PC.BD.96735 ASSY A2						A810000011
A3	PC.BD.96736 ASSY A3						A810000012
T1	HYBRID TRANS				HEYBOER	HT 3736	450100001

Table 8—5. "A" Receive Control Switch A2

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-2	.1UF		10%	600V	SPRAGUE	225P10496YD3	320001041
J1	40 PIN				3M	3432-1002	654001901
R1-2	402K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220240231
R3	604K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260431
R4	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260611
R5-6	402K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220240231
R7	604K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260431
R8	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260611
R29	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R30	470-	1/4W	10%		AB	TYPE CB	200104716
S7	PC BD MTG				LEDEX	753518-001	625000400
S8	PC BD MTG				LEDEX	753520-001	625000402
S9	PC BD MTG				LEDEX	753523-001	625000405

Table 8—6. "B" Receive Control Switch A3

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
R9	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R10	12.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212421
R11	24.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224922
R12	61.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261921
R13	124K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212431
R14	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R15	12.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212421
R16	24.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224922
R17	61.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261921
R18	124K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212431
R19	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R20	12.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212421
R21	24.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224922
R22	61.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261921
R23	124K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212431
R24	6190-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261911
R25	12.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212421
R26	24.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224922
R27	61.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261921
R28	124K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212431

Table 8—7. Battery Indicator A4

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
M1	METER,MINI,90DEG,PC MTG				EMICO	802PJR	901500100
R1	150-	1/4W	10%		AB	TYPE CB	200101516
R2	910-	1/4W	5%		A.B.	TYPE CB	200109115

Table 8—8. High Voltage A14

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
A5	PC 96746 CRT PWR,DEFL AMP						A810000029
A16	PC 96835 HIGH VOLTAGE						A810000028
XV1	TUBE SOCKET FOR 725000101				AMPEREX	55566	826400101

Table 8—9. CRT Power Supply And Deflection Amplifier A5

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-2	.01UF		20%	3KV	SPRAGUE	30GA-S10	330401030
C3	22UF		F 20%	35V	SPRAGUE	196D226X0035PE4	310802261
C7	.1UF		10%	100V	SPRAGUE	225P10491WD3	320001040
C8-9	.01UF		10%	100V	SPRAGUE	225P10391WD3	320001030
C10-11	22UF		F 20%	35V	SPRAGUE	196D226X0035PE4	310802261
C13	100MF			25V	TSI	PA100KN25NP	301301074
C17	10UF		10%	20V	SPRAGUE	150D106X9020B2	310301060
CR1-3	D035 4NS 10MA SI 50UA				FAIRCHILD	1N4148	560041480
CR4	RECTIFIER 3000VRWM				MOTOROLA	MR250-3	560002503
L1	8.2MH				MILLER	9250-825	450300502
L2-3	.1MH				MILLER	9350-32	450300501
Q1-3	TO-92 625MW TA NPN			200V	MOTOROLA	MPS-D01	550000001
Q4-5	TO-92 360MW TA NPN			30V	T.I	2N3709	550003709
Q6	TO-92 625MW TA NPN			200V	MOTOROLA	MPS-D01	550000001
Q7	TO-92 350MW TA NPN			25V	MOTOROLA	MPS6515	550065150
Q8	CASE 152	1W	TA	PNP	40E	MOTOROLA	MPS-U95
Q9	CASE 152	1W	TA	NPN	40V	MOTOROLA	MPS-U45
Q10-11	TO-92 625MW TA NPN			200V	MOTOROLA	MPS-D01	550000045
Q12-13	TO-92 350MW TA PNP			40V	MOTOROLA	MPS6518	550065180
R1	4530-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220245311
R2	5.6K	1/4W	10%		AB	TYPE CB	200105626
R3	2 K		10%		CTS	BG 42941	231802020
R4	5.6K	1/4W	10%		AB	TYPE CB	200105626
R5-6	2 K		10%		CTS	PG 42941	231802020
R7	4530-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220245311
R8-9	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R10-11	301K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230131
R12-13	3010-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230111
R14	2.5 M		10%		CTS	PG 42940	231802550
R15	10.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210721
R16	2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220011
R17-18	301K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220230131
R19	2K	.75W	10%		HELIPOT	R9PR2K	232502020
R21	2K	.75W	10%		HELIPOT	R9PR2K	232502020
R23	1MEG	.75W	10%		HELIPOT	R9PR1M	232501050
R25	15K	1/4W	10%		AB	TYPE CB	200101536
R26	1K	1/4W	10%		AB	TYPE CB	200101026
R28	330-	1/4W	10%		AB	TYPE CB	200101316
R29	130-	1/4W	5%		A.B.	TYPE CB	200102246
R30	220K	1/4W	10%		AB	TYPE CB	200101315
R33	1K	1/4W	10%		AB	TYPE CB	200101026
R34-35	220K	1/4W	10%		AB	TYPE CB	200102246
R38	75K	1/4W	5%		A.B	TYPE CB	200107535
R43	150-	1/4W	10%		AB	TYPE CB	200101516

Table 8—10. High Voltage Supply A16

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
A16	HIGH VOLTAGE SUPPLY						970096835
C1-2	.01UF		20%	3KV	SPRAGUE	30GA-S1C	330401030
CR1-2	RECTIFIER 3000VRWM				MOTOROLA	MR250-3	560002503
R1	10K	1/4W	10%		AB	TYPE CB	200101036
R2-3	1M	1/4W	10%		AB	TYPE CB	200101056
R4	3.3M	1/4W	10%		AB	TYPE CB	200103356
R5	1M	1/4W	10%		AB	TYPE CB	200101056
R6-14	3.3M	1/4W	10%		AB	TYPE CB	200103356
T1	XFMR,8100 CONVERTER				ARTTED	AC0240	420900102
U1	6DIL			86V	GE	H11A1	515000101

Table 8—11. Frequency Counter And Display A6

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-2	68PF		2%	100V	ELMENCO	CM04DA680G0	335406800
C3-7	1000PF	Z5RTC	10%	1KV	CENTRALAB	DD-102	330001020
C8-11	.01UF		00	50V	CENTRALAB	CK-103	330701030
CR1-3	D035 4NS 10MA	SI	50UA		FAIRCHILD	1N4148	560041480
CR5-6	D035 4NS 10MA	SI	50UA		FAIRCHILD	1N4148	560041480
Q1-4	Q-92 350MW TA	NPN	25V		MOTOROLA	MPS6515	550065150
R1	1M	1/4W	10%		AB	TYPE CB	200101056
R2	1K	1/4W	10%		AB	TYPE CB	200101026
R3-7	10K	1/4W	10%		AB	TYPE CB	200101036
R8-14	390-	1/4W	10%		AB	TYPE CB	200103916
R15-18	27K	1/4W	10%		AB	TYPE CB	200102736
U1	14DIP-P	B		CMOS	RCA	CD4069	510004069
U2	16DIP-P	B		CMOS	RCA	CD4020	510004020
U3	16DIP-P	B		CMOS	RCA	CD4017	510004017
U4	16 DIP			CMOS	NATIONAL	74C925	510274925
U5-6	14DIP-P	B/UB		CMOS	RCA	CD4011	510004011
U7	14DIP-P	B		CMOS	RCA	CD4069	510004069
U8	14DIP-P	B		CMOS	RCA	CD4013	510004013
U9-12	14DIL				H.P.	5082-7653	728301703
XU9-12	14 DIP RIGHT ANGLE SOCKET				ARIES	14-810-90	820101710
XY1	SKT				AUGAT	8000-DG4	826500200
Y1	XTAL,SERIES RESONANCE				CRYSTEK	HC-13,163.840KHZ	919101400

Table 8—12. Mother Board A7

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
J1-2	40 PIN				3M	3432-2002	654001902
XA8-10	TYPE 1F 22 DUAL MIL BLWS				AMPHENOL	225-22221-110	651701200

Table 8—13. Receiver A8

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-2	22UF		F 20%	35V	SPRAGUE	196D226X0035PE4	310802261
C3-4	.01UF		00	50V	CENTRALAB	CK-103	330701030
C5-6	.011UF		.5%	100V	F-DYNE	PC11-.011-100-.5	322201130
C7-8	.01UF		00	50V	CENTRALAB	CK-103	330701030
C9-12	.011UF		.5%	100V	F-DYNE	PC11-.011-100-.5	322201130
C13	300PF		2%	100V	ELMENCO	CM04DA301GO	335403010
C14	.011UF		.5%	100V	F-DYNE	PC11-.011-100-.5	322201130
C15-16	10UF		B 20%	20V	SPRAGUE	196D106X0020JA1	310801060
C17-18	.01UF		00	50V	CENTRALAB	CK-103	330701030
C19	2.2UF	Y5V TC	20%	50V	ERIE	8141-050-651-225M	330802250
C20-21	.22UF	Y5V TC	20%	50V	ERIE	8131-050-651-224M	330802240
C22	560PF		2%	100V	ELMENCO	CM06DA561GO	335405610
C23	30PF		2%	500V	ELMENCO	CM04-D300GO	335403000
C24	.011UF		.5%	100V	F-DYNE	PC11-.011-100-.5	322201130
C25-33	.01UF		00	50V	CENTRALAB	CK-103	330701030
C34-35	2.2UF	Y5V TC	20%	100V	USCC	CY50A225M	330802251
CR1-6	D035 4NS 10MA		SI	50UA	FAIRCHILD	1N4148	560041480
CR9-18	D035 4NS 10MA		SI	50UA	FAIRCHILD	1N4148	560041480
CR21-22	D07	.25W	5%	6.2V	DICKSON	1N823	563008230
G1	TO-92 360MW TA	NPN		30V	T.I	2N3709	550003709
G2	MODTO92 360MW TA	N		30V	T.I.	T1S73	554000730
G3-6	TO-92 360MW TA	NPN		30V	T.I	2N3709	550003709
G7	MODTO92 360MW TA	N		30V	T.I.	T1S73	554000730
G8	TO-92 360MW TA	NPN		30V	T.I	2N3709	550003709
G9-10	MET.CAN 500MW TA	NPN		60V	TI	2N2920	550002920
R1-2	121K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212131
R3	11.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211821
R4	11K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211021
R5	2K	.75W	10%		HELIPOT	89PR2K	232502020
R6	12.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212121
R7	76.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220276821
R8	9530-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220295311
R9	18.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218721
R10	37.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237421
R11	18.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218721
R12	37.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220237421
R13	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R14	162-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216201
R15	27K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227021
R16	11K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211021
R17	26.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226721
R18	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R19	162-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216201
R20-21	8.06K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220280611
R22	15.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215821
R23-24	499-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220249901
R25-26	26K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226021
R27	54.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220254921
R28-29	1500-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215011
R30	6.8K	1/4W	10%		AB	TYPE CP	200106826
R31	1M	1/4W	10%		AB	TYPE CB	200101056

Table 8—13. (cont'd)

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
R32	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R33	3160-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231611
R34	59.8K	1/8W	.25		ELECTRA	RN55 SIZE 100 PPM	220459828
R35	604-	1/8W	.25		ELECTRA	RN55 SIZE 100 PPM	220460408
R36	1.953K	1/8W	.25		ELECTRA	RN55 SIZE 100 PPM	220419518
R37	6.644K	1/8W	.25		ELECTRA	RN55 SIZE 100 PPM	220466418
R38	27.655K	1/8W	.25		ELECTRA	RN55 SIZE 100 PPM	220427628
R39-40	15K	1/4W	10%		AB	TYPE CB	200101536
R41-42	3160-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220231611
R43	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R44	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R45	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R46	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R47	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R48	68.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220268121
R49	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R50	20K	.75W	10%		HELIPOT	89PR20K	232502030
R51	102K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210231
R52	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R53	267K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220226731
R54	19.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219121
R55	75K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220275021
R56	93.1K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220293121
R57	46.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220246421
R58	20K	.75W	10%		HELIPOT	89PR20K	232502030
R59	6810-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220268111
R60	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R61	5110-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220251111
R62	1150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211511
R64	2K	1/2W	10%	200V	HELIPOT	72PMR2K	232702020
R65-66	33.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233221
R67	32.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220232421
R68	4750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220247511
R69-70	249K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224931
R71	1K	3W	1%		TEL LABS	QR1 1000 OHMS	211510011
R72	6040-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260411
R73	2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220011
R74	50K	1/2 W	10%	200V	HELIPOT	72PMR50K	232705032
R75	9.31K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220293111
R76	4750-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220247511
R77	1M	1/4W	10%		AB	TYPE CB	200101056
R78	30K	1/4W	5%		AB	TYPE CB	200103035
R79-80	33K	1/4W	10%		AB	TYPE CB	200103336
R81	10K	1/4W	10%		AB	TYPE CB	200101076
R82	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R83	1000-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210011
R84	121K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220212131
U1-3	14 DIP				RAYTHEON	RC4136DB	500004136
U4	8DILP				NATIONAL	LM308N	500003080
U5	14 DIP				RAYTHEON	RC4136DB	500004136
XU2	14PDIL				ROB NUGENT	ICL-143-S6-G	620100300

Table 8—14. Transmitter A9

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1-2	22UF		F	20% 35V	SPRAGUE	196D226X0035PE4	310802261
C3-4	.01UF		00	50V	CENTRALAB	CK-103	330701030
C5	22UF		F	20% 35V	SPRAGUE	196D226X0035PE4	310802261
C6-7	.01UF		00	50V	CENTRALAB	CK-103	330701030
C8	.039UF		1%	100V	F-DYNE	PPT11-.0391001	322303931
C9-10	2.2UF	Y5V	TC 20%	50V	ERIE	8141-050-651-225M	330802250
C11-12	2000PF		2%	100V	ELMENCO	CM06DA202G0	335402020
C13-14	1200PF		2%	100V	ELMENCO	CM06DA122G0	335401220
C15-16	.01UF		00	50V	CENTRALAB	CK-103	330701030
C17	1000PF		2%	100V	ELMENCO	CM06DA102G0	335401020
C18-20	2000PF		2%	100V	ELMENCO	CM06DA202G0	335402020
C21-22	1000PF		2%	100V	ELMENCO	CM06DA102G0	335401020
C23	300PF		5%	500V	ELMENCO	CM15-E301J	335003010
C24	.01MF		1%	100V	F-DYNE	PPT11-.01-100-1	322301031
C25	.47UF	Y5V	TC 20%	50V	ERIE	8131-050-651-474M	330804740
C26	.1UF	Y5V	TC 20%	50V	ERIE	8121-050-651-104M	330801040
C27	.22MF		1%	100V	F-DYNE	PPT11-.22-100-1	322302241
C28-31	22UF	F	20% 35V		SPRAGUE	196D226X0035PE4	310802261
C32-33	.01UF		00	50V	CENTRALAB	CK-103	330701030
C34	22UF	F	20% 35V		SPRAGUE	196D226X0035PE4	310802261
C35	.039UF		1%	100V	F-DYNE	PPT11-.0391001	322303931
C36	300PF		5%	500V	ELMENCO	CM15-E301J	335003010
C37-39	.01UF		00	50V	CENTRALAB	CK-103	330701030
C40	22UF	F	20% 35V		SPRAGUE	196D226X0035PE4	310802261
C41	.22MF		1%	100V	F-DYNE	PPT11-.22-100-1	322302241
C42	.01UF		00	50V	CENTRALAB	CK-103	330701030
C43	.15UF		1%	100V	F-DYNE	PPT11-.15-1001	322301541
C44	2000PF		2%	100V	ELMENCO	CM06DA202G0	335402020
C45	2.2UF	Y5V	TC 20%	50V	ERIE	8141-050-651-225M	330802250
C46-47	.01UF		00	50V	CENTRALAB	CK-103	330701030
C48	22UF	F	20% 35V		SPRAGUE	196D226X0035PE4	310802261
C49-50	.1UF	Y5V	TC 20%	50V	ERIE	8121-050-651-104M	330801040
C51	100PF		2%	500V	ARCO	CM04FD101G0	335401010
C52	.1UF	Y5V	TC 20%	50V	ERIE	8121-050-651-104M	330801040
C53	.01UF		00	50V	CENTRALAB	CK-103	330701030
C55	.47UF	Y5V	TC 20%	50V	ERIE	8131-050-651-474M	330804740
C56	2.2UF	Y5V	TC 20%	50V	ERIE	8141-050-651-225M	330802250
CR1-14	D035 4NS 10MA		SI	50UA	FAIRCHILD	1N4148	560041480
G1	TO-92 360MW TA	PNP		30V	T.I.	2N4059	552004059
G2	TO-92 360MW TA	NPN		30V	T.I	2N3709	550003709
G3	TO92 310MW TA	P		60V	MOTOROLA	2N5463	555005463
G4-22	TO-92 360MW TA	NPN		30V	T.I	2N3709	550003709
G23	TO-92 360MW TA	PNP		30V	T.I.	2N4059	552004059
R1	62K	1/4W	10%		A.B.	TYPE CB	200106236
R2	5.62K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256211
R3	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R4	1K	1/4W	10%		AB	TYPE CB	200101026
R6-8	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R9	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R10	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210021
R11	56.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256221

Table 8—14. (cont'd)

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
R12-14	1K	.75W	10%		HELIPOT	89PR1K	232501020
R15	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R16	100K	.75W	10%		HELIPOT	89PR100K	232501040
R17-18	2430-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220224311
R19	4.7M	1/4W	10%		AB	TYPE CB	200104756
R20	100K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210031
R21	23.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223721
R22	9090-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220290911
R23	47K	1/4W	10%		AB	TYPE CB	200104736
R24	15K	1/4W	10%		AB	TYPE CB	200101536
R25	430K	1/4W	10%		AB	TYPE CB	200104346
R26	470-	1/4W	10%		AB	TYPE CB	200104716
R27	15K	1/4W	10%		AB	TYPE CB	200101536
R28	110K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211031
R30	470-	1/4W	10%		AB	TYPE CB	200104716
R31	54.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220254921
R32-33	365K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220236531
R34	182K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218231
R35	324K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220232431
R36	332K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220233231
R37	39K	1/4W	10%		AB	TYPE CB	200103936
R38-39	56.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220256221
R40	287K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228731
R41	470-	1/4W	10%		AB	TYPE CB	200104716
R42	16.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216921
R43-44	34K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234021
R45	1430-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214311
R46	287K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228731
R47	392K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220239231
R48	15K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215021
R49-50	1M	1/4W	10%		AB	TYPE CB	200101056
R51	15K	1/4W	10%		AB	TYPE CB	200101536
R52	34.8K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234821
R53	30K	1/4W	5%		AB	TYPE CB	200103035
R54	33K	1/4W	10%		AB	TYPE CB	200103336
R55	30K	1/4W	5%		AB	TYPE CB	200103035
R57	1430-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220214311
R58	16.9K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216921
R59	27K	1/4W	10%		AB	TYPE CB	200102736
R60	8660-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220286611
R61	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220021
R62-63	1K	.75W	10%		HELIPOT	89PR1K	232501020
R64	82.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220282521
R65	1M	1/4W	10%		AB	TYPE CB	200101056
R66	1K	1/4W	10%		AB	TYPE CB	200101026
R67	10K	1/4W	10%		AB	TYPE CB	200101036
R68	4.7K	1/4W	10%		AB	TYPE CB	200104726
R69	10K	1/4W	10%		AB	TYPE CB	200101036
R70-71	4.7K	1/4W	10%		AB	TYPE CB	200104726
R72	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R73	200-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220220001
R74-75	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R76	220K	1/4W	10%		AB	TYPE CB	200102246
R77	20K	.75W	10%		HELIPOT	89PR20K	232502030

Table 8—14. (cont'd)

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
R78	42.2K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220242221
R79	95.3K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220295321
R80	11K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220211021
R81-96	10K	1/4W	10%		AB	TYPE CB	200101036
R97	1.5K	1/4W	10%		AB	TYPE CB	200101526
R98	35.7K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220235721
R99-100	10.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220210521
R101	16.5K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220216521
R102	5490-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220254911
R103	7.32K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220273211
R104	3480-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220234811
R105	4320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243211
R106	2370-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223711
R107	4320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243211
R108	2870-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220228711
R109	59K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220259021
R110	13K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220213021
R111	1960-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220219611
R112	9760-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220297611
R113	27.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220227421
R114	6650-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220266511
R115	60.4K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220260421
R116	20K	1/4W	5%		AB	TYPE CB	200102035
R117-118	180-	1/4W	10%		AB	TYPE CB	200101816
R119-120	15K	1/4W	10%		AB	TYPE CB	200101536
R121-122	1M	1/4W	10%		AB	TYPE CB	200101056
U1	14 DIP				RAYTHEON	RC4136DE	500004136
U2	8PDIL				NAT. SEMI	LM741CN	500007412
U3	14DILP				INTERSIL	SEE SPECS.	516200200
U4	14 DIP				RAYTHEON	RC4136DB	500004136
U5	14 DIP				RAYTHEON	RC4136DE	500004136
U6	8PDIL	80MW		180	SIGNETICS	N5558V	500055580
U7	8DIP-PM			LM	SIGNETICS	SE555V	510000555
U8	8PDIL	80MW		180	SIGNETICS	N5558V	500055580
XU3	14PDIL				ROB NUGENT	ICL-143-S6-G	820100300

Table 8--15. Digital Memory A10

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	M.E.C. PART NO.
C1	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C2	.1UF	Y5V	TC 20%	50V	ERIE	8121-050-651-104M	330801040
C3	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C4	.01UF		00	50V	CENTRALAB	CK-103	330701030
C5	1000PF	Z5R	TC 10%	1KV	CENTRALAB	DD-102	330001020
C6-8	.01UF		00	50V	CENTRALAB	CK-103	330701030
C9	68PF		2%	100V	ELMENCO	CM04CA680GO	335406800
C10-13	.01UF		00	50V	CENTRALAB	CK-103	330701030
C14	.1UF	Y5V	TC 20%	50V	ERIE	8121-050-651-104M	330801040
C15	.01UF		00	50V	CENTRALAB	CK-103	330701030
C16	22UF	F	20%	35V	SPRAGUE	196D226X0035PE4	310802261
C17-22	.01UF		00	50V	CENTRALAB	CK-103	330701030
C23	68PF		2%	100V	ELMENCO	CM04CA680GO	335406800
C24	100PF		2%	500V	ARCO	CM04FD101GO	335401010
C25	300PF		2%	100V	ELMENCO	CM04CA301GO	335403010
CR1-6	D035 4NS 10MA		SI	50UA	FAIRCHILD	1N4148	560041480
G1-4	TO-92 360MW TA		PNP	30V	T.I.	2N4059	560040C59
R1	100K	1/4W	10%		AB	TYPE CB	200101046
R2	1M	1/4W	10%		AB	TYPE CB	200101056
R3	1K	1/4W	10%		AB	TYPE CB	200101026
R4	4.7K	1/4W	10%		AB	TYPE CB	200104726
R5	220-	1/4W	10%		AB	TYPE CB	200102216
R6	10K	1/4W	10%		AB	TYPE CB	200101036
R7	390-	1/4W	10%		AB	TYPE CB	200103916
R8-9	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	200220021
R10-12	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	200210021
R13	10K	1/4W	10%		AB	TYPE CB	200101036
R14-15	6.8K	1/4W	10%		AB	TYPE CB	200106826
R16-17	20K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	200220021
R18	10K	1/4W	10%		AB	TYPE CB	200101036
R19	1.8K	1/4W	10%		AB	TYPE CB	200101826
R20	10K	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	200210021
R21-32	10K	1/4W	10%		AB	TYPE CB	200101036
R33	33K	1/4W	10%		AB	TYPE CB	200103336
R34	10K	1/4W	10%		AB	TYPE CB	200101036
R35	33K	1/4W	10%		AB	TYPE CB	200103336
R36	10K	1/4W	10%		AB	TYPE CB	200101036
R37	10K	1/4W	10%		AB	TYPE CB	200101036
R38	1.8K	1/4W	10%		AB	TYPE CB	200101826
R39	2.7K	1/4W	10%		AB	TYPE CB	200102726
U1	16DIP-P		B		CMOS MOTOROLA	MC14028	510004028
U2	16DIP-P		B		CMOS RCA	CD4050	510004050
U3	14DIP-P		B		CMOS RCA	CD4068	510004068
U4	14DIP-P	B/UB			CMOS RCA	CD4011	510004011
U5	14DIP-P		B		CMOS RCA	CD4013	510004013
U6	16DIP-P		B		CMOS RCA	CD4020	510004020
U7	14DIP-P		B		CMOS RCA	CD4013	510004013
U8	16 DIP				ANALOG DEV	AD7530JN	510100201
U9	14DIP-P		B		CMOS RCA	CD4013	510004013
U10	14 DIP				RAYTHEON	RC4136CB	500004136
U11	14DIP-P		B		CMOS RCA	CD4013	510004013
U12	16 DIP				ANALOG DEV	AD7530JN	510100201
U13	16DIP-P		B		CMOS RCA	CD4019	510004019
U14	16DIP-P		B		CMOS RCA	CD4049	510004049
U15	16DIP-P		B		CMOS RCA	CD4019	510004019
U16	14DIP-P	B/UB			CMOS RCA	CD4011	510004011
U17-18	8DIP-P				MOS SIGNETICS	2503V	510025030
U19	16DIP-P		B		CMOS RCA	CD4019	510004019
U20-21	8DIP-P				MOS SIGNETICS	2503V	510025030
U22	14DIP-P	B/UB			CMOS RCA	CD4023	510004023
U23-24	14DIP-P	B			CMOS RCA	CD4013	510004013
U25	16DIP-P	B			CMOS RCA	CD4049	510004049
Y1	CRYSTAL SKT MTG				VALPEY	VR6-1.544MHZ	919100500

Table 8—16. Power Supply A11

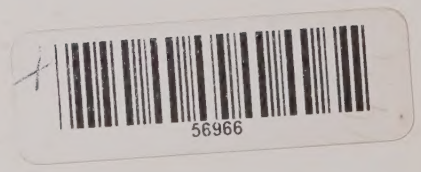
REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
C1	100PF		2%	500V	ARCO	CM04FD101G0	335401010
C2	22UF		F 20%	35V	SPRAGUE	196D226X0035PE4	310802261
F1	FUSE 3AG				LITTELFUSE	3AG	863100600
PS2	150MA		+-	15V	S.-ARNOLD	A6/D15/150/Z	960100002
Q1	TO-66	25W	TC	NPN 55V	RCA	2N3054	550030540
R1	100-	3W	5%		W LEONARD	TYPE 3X	210301015
R2	1-	3W	5%		W LEONARD	TYPE 3X	210300105
R3	1540-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220215411
R4	4320-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220243211
R5	1820-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220218211
R6	1K	.75W	10%		HELIPOT	89PR1K	232501020
U1	10PT05				FAIRCHILD	UA723HC	500077230
XF1	3AG				LITTELFUSE	102069	863300300

Table 8—17. Power Supply A11PS1

	VALUE	POWER	TOL	VOLTS	DESCRIPTION
C1	100 UF			35V	Electrolytic capacitor
C2	9000 UF			15V	Electrolytic capacitor
C3	.001 UF			100V	Film capacitor
C4	100 UF			35V	Electrolytic capacitor
CR1-2	AE3B			100V	3Amp diode
CR3-5	AE1C			200V	1Amp diode
R1	2.2K	½W	5%		Carbon film resistor
R3	330	½W	5%		Carbon film resistor
R4	47	½W	5%		Carbon film resistor
R7	0.12	¼W	2%		Metal film resistor
R8	2.2K	½W	5%		Carbon film resistor
R9	6.8	½W	5%		Carbon film resistor
R10	2.2K	½W	5%		Carbon film resistor
R11	1.5K	2W	5%		Carbon film resistor
R12	2.2K	½W	5%		Wire wound potentiometer
R13	1.6K	¼W	2%		Carbon film resistor
R15-17	6.8	½W	5%		Metal film resistor
Q1	2N3055				Power transistor
Q2	2N2219A				Signal transistor
U1	Ua 723				IC voltage regulator
T1	11023				Power transformer

Table 8—18. Front Panel A15

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E.C. PART NO.
A1	PC.BD.96734 ASSY A1						A810000010
A4	PC.BD.96759 ASSY A4						A810000013
A13	RECEIVE CONTROL SW.A13						A810000023
DS1	LED,RED DIFF,PANEL				MONSANTO	MV5023	564500900
F1	FUSE 3AG				LITTELFUSE	3AG	863100300
J1	BINDING POST-RED				GRAYHILL	29-1R	652400400
J1	SKT MATE-N-LOCK LOOSE				AMP	60617-1	863400300
J2	BINDING POST-BLK				GRAYHILL	29-1B	652400300
J3	BINDING POST-RED				GRAYHILL	29-1R	652400400
J4	BINDING POST-BLK				GRAYHILL	29-1B	652400300
J5	BINDING POST-RED				GRAYHILL	29-1R	652400400
J6	BINDING POST-BLK				GRAYHILL	29-1B	652400300
J7	BINDING POST-RED				GRAYHILL	29-1R	652400400
J8	BINDING POST-BLK				GRAYHILL	29-1B	652400300
J9	BINDING POST METAL GND				H H SMITH	137SP	652500100
J11	3-PIN	6A		250V	BELDEN	17252	652201700
MP1	DISPLY BEZEL W/NEUTRAL FL				NOBEX	910-15	857000301
P1	2 COND				AMP	1-480318-0	650900200
P1	SKT MATE-N-LOCK LOOSE				AMP	60617-1	863400300
R2	2K-10K		30%		CTS	LM 2773	233102020
S1	SPDT	6A		125V	ALCO	MTG-106E	620402903
S6	SPDT	6A		125V	ALCO	MTG-106E	620402903
S10-12	SPDT	6A		125V	ALCO	MTG-106D	620402902
S13-14	SPDT	6A		125V	ALCO	MTG-106E	620402903
S15	SPDT	6A		125V	ALCO	MTG-106D	620402902
XF1	FUSE HOLDER PANAL MTG				BUSSMAN	BUSS HTA	863300010



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